Instruction manual

FPLA PROGRAMMER X

026-6610
REV B MARCH, 80

901-6610

DATA I/O

Programming systems for tomorrow...today

FPLA PROGRAMMER X

026-6610
REV B MARCH, 80

901-6610

TABLE OF CONTENTS

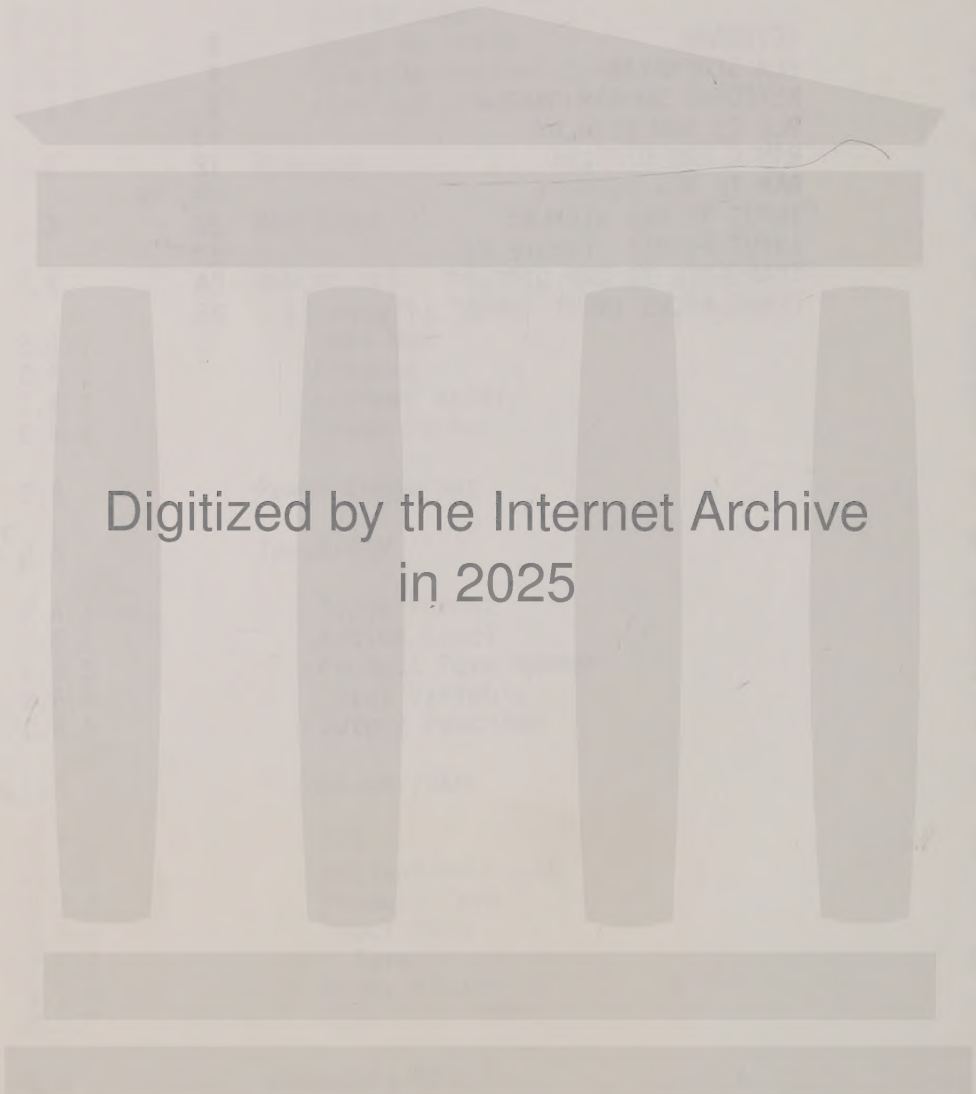
MODEL $\overline{X}$ OPERATOR'S MANUAL

SECTION		PAGE
	INTRODUCTION	
	IMPORTANT NOTICE	
1.0	GENERAL DESCRIPTION	1
1.1	Power Source	1
1.2	Installation Instructions	1
1.3	Card Removal	2
1.4	Front Panel Controls and Indicators	2
1.4.1.	Mode Controls	3
1.4.1.0	List	3
1.4.1.1	Input/RAM	3
1.4.1.2	Translator/RAM	3
1.4.1.3	Keyboard/RAM	3
1.4.1.4	PLA/RAM	3
1.4.1.5	RAM Clear	4
1.4.1.6	RAM-PLA	4
1.4.1.7	RAM-Output	4
1.4.2	Function Controls	4
1.4.2.1	Auto/Manual	4
1.4.2.2	Test New	4
1.4.2.3	Program	4
1.4.2.4	Logical Verify	5
1.4.2.5	Array Verify	5
1.4.2.6	Stop/Start	5
1.4.3	Keyboard	5
1.4.3.1	Cursor Control	5
1.4.3.2	Data Keys	6
1.4.4	CRT Display	6
1.5	Terms	7
1.5.1	PLA	7
1.5.2	Product Term	7
1.5.3	Input Variable	8

1.5.4	Output Function	8
1.5.5	Active Level	8
1.5.6	CRT	8
2.0	OPERATING INSTRUCTIONS	9
2.1	Keyboard/RAM	9
2.1.1	Active Level	9
2.1.2	Input Variable	9
2.1.3	Skipping Product Terms	10
2.1.4	Clearing a Product Term	10
2.2	PLA/RAM	10
2.3	RAM/CLEAR	10
2.4	RAM to PLA	12
2.4.1	Test New	13
2.4.2	Program	13
2.4.3	Logical Verify	13
2.4.4	Array Verify	13
2.5	Power Interrupt	14
2.6	Input/RAM	17
2.6.1	Input Format	17
2.6.2	Active Level	17
2.6.3	Product Term Number	18
2.6.4	Input Variable	18
2.6.5	Output Function	20
2.7	Translator/RAM	21
2.7.1	STX	21
2.7.2	Activation Level	21
2.7.3	Product Term	26
2.7.4	Input Term	26
2.7.5	F Term	26
2.7.6	Error Fields	26
2.7.7	ETX	27
2.8	Signetics FPLA	28

LIST OF ILLUSTRATIONS

KEYBOARD	5
PLA SCHEMATIC	7
KEYBOARD TO RAM DISPLAY	9
PLA TO RAM DISPLAY	11
RAM CLEAR DISPLAY	12
RAM TO PLA DISPLAY	15, 16
INPUT TO RAM DISPLAY	22
INPUT FORMAT (figure 6)	23
TRANSLATE TO RAM DISPLAY	24
TRANSLATING INPUT FORMAT (figure 7)	25


Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_10299

DATA I/O MODEL X

FPLA PROGRAMMER

INTRODUCTION

The DATA I/O Model X FPLA Programmer is an instrument which has the capability of programming FPLA (FIELD PROGRAMMABLE LOGIC ARRAY) devices. The FPLA is a unique device different from a PROM in both its application and programming characteristics. A completely new instrument is required to allow programming of the FPLA because of the unique differences involved. The Model X FPLA Programmer has the capability of programming the devices from an input source of Punch Paper Tape, Mark Sense Cards, Parallel Remote Input Interface, or Copy Mode Master to Slave. (1)

Different manufacturers of FPLA devices have different architecture for the devices in both Pinout configuration and Input Variable size. The basic FPLA device contains 48 product terms and from 14 to 16 Input variables, (I Terms), 8 Output functions (F Terms), and 8 Output activation level selections. The different manufacturer's FPLA devices may be programmed in the Model X Programmer by use of a three card Personality Set. Expanded versions will be available when Product Term sizes arrive at 96 or higher levels.

Due to the complexity of the internal data routing of an FPLA Programmer, a CRT (Viewable screen) is implemented into the Programmer to inform the operator more completely the data levels and modes of operation taking place within the Programmer.

The CRT is used to inform the operator as to the data being presented from the RAM Memory for a given Product Term number, and all of the presented variables for both the I Term, F Term,* and activation level. As the PLA is updated to these levels, the screen informs the operator as to the progress and if an error occurred in any sector of the programming or verification sequence, the information is clearly displayed on the screen for the operator to diagnose or take appropriate action.

Minimum switches and indicators are used on the control panel of the Model X and are completely interlocked to prevent inadvertent errors due to operator intervention at a wrong or inappropriate time.

* F Term and Output Function are used interchangably.

1 See section 1.5 for PLA explaination.

IMPORTANT NOTICE

PLA MUST BE REMOVED FROM THE MASTER SOCKET WHEN POWER IS TURNED OFF AND ON.

DEVICE DAMAGE MAY RESULT IF PLA IS LEFT IN SOCKET DURING THIS TIME.

1.0 GENERAL DESCRIPTION

The Model $\overline{X}$ Programmer is designed to program FPLA's of several manufacturers by simply replacing the personality modules inside the Programmer. A cathode ray tube (CRT) display is used as a data interface between the operator and the Programmer. Diagnostic information is displayed at the bottom of the CRT to indicate the status of the Programmer's operation.

A Paper Tape Reader is used as a standard, integral input data source in the Model $\overline{X}$ Programmer. Also standard is a keyboard which is used for entering information manually and to control the display on the CRT as the operator desires.

1.1 POWER SOURCE

The Model $\overline{X}$ Programmer operates from input power sources of 100, 120, 200, 240 Volts AC, 50/60 Hz. Selection of input power is made on the rear panel by removing the power cord and sliding the fuse protective cover to the UP position. A small printed circuit card is contained in the left section of the power cord socket which has the indicated voltage level showing visibly from the rear. By rotating the printed card and inserting it into the receptacle for the desired input power source, the power source may be changed in the field. However, the power is normally set at the factory for the desired voltage depending on the destination of the Programmer.

1.2 INSTALLATION INSTRUCTIONS

When receiving the Model $\overline{X}$, the carton must first be inspected for visible shipping damage. The Model $\overline{X}$ Programmer is contained in a heavy carton with foam cushions supporting it for maximum protection during shipment. If the box has been compressed or severely dented or broken, care must be taken to insure that the proper insurance claim procedures are followed.

Once the carton has been opened, remove the Programmer from the carton and notice that the top cover of the Programmer does not contain the CRT. It is separately packed in another container for maximum shipping protection.

Remove the top cover by depressing the buttons on either side of the cover assembly. By moving the cover in a vertical direction, the cover may be easily removed. (1)

Unpack the CRT from its separate shipping enclosure, and notice that there are two flat ribbon connectors extending from the bottom of the CRT unit. Place the two connectors through the mounting hole in the top of the Model $\overline{X}$ top cover. With the four screws and washers enclosed with the CRT unit, mount the unit to the appropriate mounting holes with the CRT facing in the forward direction. The mounting screws are inserted from the bottom of the top cover.

(1) CRT may be packed with TOP COVER attached. It will be packed in a separate shipping carton for safety.

With the four mounting screws securely in place, the CRT is now a physical part of the top cover assembly. The two cables are now attached to the appropriate locations.

1. The short cable marked J-4 is inserted into the appropriate connector assembly of the small Main Electronic Unit (MEU) attached to the top cover assembly. This is found by placing the top cover in the vertical position with the CRT face pointing up. The three small cards associated with the CRT control are then located to the left center of the top cover. J-4 is located in the MEU in the lower left hand corner. Observe polarity so that the stripe of the J-4 attaching connector is to the inside of the MEU marked by a "dot".

2. The two cables exiting from the CRT itself through the mounting hole are routed under the card cage mounted on the top cover by first loosening the four mounting nuts, sliding the cables underneath the mother board and then retightening the nuts once again.

3. The second connector (longest cable) is connected to the mother board of the Model $\overline{X}$ Programmer labeled CRT Data (J-4). The other cable exiting from the top cover is a 3 conductor power cable which inserts into the appropriate colored connector attached to the main MEU of the Programmer. Once these connectors are in place, the top cover is complete.

While the top cover is removed from the Programmer, inspect that all connectors and cards are firmly seated and that the Reader Cable is connected firmly and that no physical damage is apparent. Once this has been accomplished, carefully insert the top cover onto the Programmer so that the two mounting buttons snap securely shut.

1.3 CARD REMOVAL

In order to remove a card from the main MEU of the Programmer first turn main power OFF and remove the top cover. Since cables are connected from the top cover CRT and appropriate control system to the main MEU of the Programmer, care must be taken when removing the top cover that it is set aside close enough that cables are not pulled from their receptacles. The cards may then be removed from the MEU by pushing the appropriate extractor ear to move the card in a vertical direction at which time it may be easily removed. Changing personality card sets to reconfigure the Programmer from one type device to another is accomplished by removing the front three cards of the main MEU. When inserting new card sets, ensure that the appropriate cables are aligned and inserted correctly, with the red stripe (Pin 1) on the cable at the left side of the connector.

1.4 FRONT PANEL CONTROLS AND INDICATORS

The Model $\overline{X}$ Programmer contains interlocked mode selector switches on the control panel, which allow the operator to select a desired input source of data and the respective output recipient. There are only two recipients of information: RAM and PLA. All preparation modes of operation are used

to input information to the RAM Buffer for storage and only one output mode is available which allows the RAM Buffer to present the information to the PLA itself. The mode switches are interlocked so that only one mode may be selected at a time. Selection may only occur in a STOP condition. This prevents inadvertent operator errors which could cause an expensive component to be ruined.

Referring to the Programmer drawing on the front page showing the front panel, it is noted that the front panel is divided into four separate categories, or sections. The front display panel area is completely blank containing only the power ON and OFF switch. This switch controls all of the power to the Model X Programmer and when placed in the ON condition, turns power on and causes an automatic reset to occur within the system. Power ON is indicated by the STOP and Manual indicators being on.

4.1 MODE CONTROLS

The Mode control section consists of four lever action dual-function switches, which may be activated only when the Programmer is in a STOP condition. This prevents inadvertent mode changing while the system is running which could cause errors. The upper right mode switch is a reset position which causes the system to completely reset. It is not a mode, but is positioned in the mode switch section for ease of operation. The selectable modes are as follows:

4.1.0 LIST

This mode is used to verify that a Translate(ASCII) coded tape has been generated properly. The ASCII characters on the tape will appear on the CRT screen without being loaded into RAM.

4.1.1 INPUT/RAM

This mode is used to accept data in machine language (Special coding) from any input source associated with the Paper Tape Reader or remove input option and store that data in the RAM Buffer. The standard input source is punched paper tape using the integral paper tape reader. If, however, Mark Sense Cards or Remote Computer Interface are used, then the appropriate selection of that remote option deselects the Reader and allows that device to input data on command.

4.1.2 TRANSLATOR/RAM

This is the Translator Input Format Mode which allows any input source to present information to the Programmer in a special translatable format. This format will be discussed under section 2.1.2 of the Manual. The data is translated from the special format into machine language and then stored in the resident RAM of the Programmer.

4.1.3 KEYBOARD/RAM

This is the manual preparation mode of operation which activates the integral keyboard. The keyboard data entry will be explained under section 2.1.3 of the Manual.

4.1.4 PLA/RAM

This mode of operation copies the contents of an existing pre-programmed PLA device of the same technology into the resident RAM Buffer of the Programmer. All information contained in the PLA is changed to machine language format so that a new device may be programmed appropriately from that information.

1.4.1.5 RAM/CLEAR

This mode of operation is a start-up feature which allows the RAM to be completely cleared upon command. The purpose of RAM/CLEAR is to allow the operator to program a single section or Product Term of a PLA device. To do this, the RAM memory must be cleared so that extraneous bits of information will not be programmed inadvertently.

1.4.1.6 RAM/PLA

This is the mode which actually programs the PLA from data contained the the RAM.

1.4.1.7 RAM/OUTPUT

This mode is used to output the data in RAM to a teletype or RS232 receiver in serial or in parallel to a remote punch. To operate, the I/O Interface board (701-1245) must be inserted into the reader driver board slot (701-1111).

1.4.2 FUNCTION CONTROLS

Six momentary push-buttons are located on the bottom center of the front panel of the Model X for Function selection. Functions are selectable only when the system is in a STOP condition to prevent inadvertent operator errors by prohibiting function changes during Programmer operation. The Function selections are defined as follows:

1.4.2.1 AUTO/MANUAL

This two-Position push-button allows the Programmer to be placed in a Manual or Auto mode of operation. The Manual mode is automatically selected when in the Keyboard mode. The operator has no control over the push-button at that time. All other modes of operation may be selected for either Manual or Auto operation. In the Manual Mode, the Programmer will halt at the end of each completed Product Term. In the Auto Mode, the Programmer will continue through all selections of functions until the End of Program occurs, at which STOP will be indicated. Complete and other responses will be displayed on the CRT. If the Programmer is in either the Input or Translate to RAM mode and Program and Auto are selected, the RAM automatically will be cleared prior to data entry from paper tape. If Program and Manual or Array Verify and either Auto or Manual is selected, the RAM will not be cleared prior to data entry.

1.4.2.2 TEST/NEW

This switch is applicable only in the RAM to PLA mode of operation, and allows the test of a PLA to determine if the device is new. The control system searches through the PLA when this mode is selected and stops at the end of the search procedure indicating on the display panel (CRT) whether the device is new or not.

1.4.2.3 PROGRAM

The Program Key may be depressed in any mode of operation. This allows data to be programmed from a selected Input data source to RAM, or from the Ram to PLA.

1.4.2.4 LOGICAL/VERIFY

Logical Verify is selectable only in the RAM to PLA mode. Depressing the switch in any other mode will not allow the indicator to remain illuminated when the switch is released.

1.2.4.5 ARRAY/VERIFY

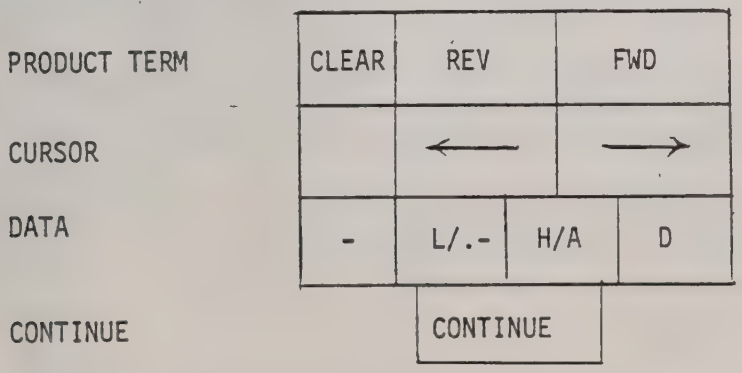
The Array Verify mode of operation is selectable in any mode. This selection allows the contents of an input source to be compared to the output recipient. This selection may be used with : Input to RAM, Translator to RAM, PLA to RAM, or RAM to PLA modes.

1.2.4.6 START/STOP

The Start/Stop switch is momentary key switch which selects the Start or initiating mode of operation, and may be selected to Halt the mode at any position. While the system is in a Start condition, no other switch may be activated on the Mode or Function control, since they are completely locked out for protection.. An automatic reset occurs when the machine is in the stopped condition and the Stop/Start switch is depressed.

1.4.3 KEYBOARD

The Keyboard is active if Keyboard/RAM mode is selected. The Keyboard is divided into four distinct zones of control



1.4.3.1 PRODUCT TERM KEYS

Three Keys control Product Term selection.

CLEAR
This Key clears the Product Term data being displayed and returns the Cursor to the first entry of the Input Term.

REV
This Key, when depressed, causes the Product Term number to be decremented by one and the display to be updated.

FWD
This Key when depressed, causes the Product Term number to be incremented by one and the display to be updated.

1.4.3.2 CURSOR CONTROL

Data may be entered onto the CRT only in the area where a Cursor is positioned. The Cursor is available only in data entry areas of: Input Variable, Output Func and Activation level. The cursor may be moved to the left or to the right by pushing the ⟵ or ⟶ key on the key panel. The Cursor may not move in a reverse direction past a limit, or in a forward direction from one Product Term to another. Therefore, the Cursor control remains in an existing Product Term on the display panel. If either key is held depressed, the Cursor will repeat step within the Product Term.

Foward (⟶) will slew thru both Input variable and Output function fields. Reverse (⟵) will slew within the limits of the field.

.4.3.3 DATA KEYS

Four Data Keys are located on the key panel which manually enter data into the appropriate section of memory and onto the CRT. These keys are dual-function keys depending upon whether an Active level, Input Variable or Output Function being used. In the Input Term mode, the keys -, L, H, and D are used to enter the appropriate information from a prepared code sheet at the Cursor position indicated on the display panel. In the Output function, the lower section of the keys are used to indicate an Active (A) or an Inactive (-) entry to the eight Output Terms. Certain PLA technologies use . (period) instead of - (dash). The CRT will display the appropriate symbol.

The Activation Level must be entered first, prior to any other entry, and uses the center two keys L and H to set the High and Low configuration of the activation level sequence.

The Continue Key is used in other modes of operation other than the keyboard mode when Manual is selected. The system may be restarted after a manual halt has occurred by pressing the Continue Key. Continue is also used to manually halt the machine while depressed.

1.4.4 CRT DISPLAY

The CRT, located on top of the Programmer, is used to communicate with the operator all appropriate information that is contained in a Product Term under test. Modes of operation are displayed as well as all Input Variables, Output Function, Activation Levels, etc. informing the operator as to the progress of the Programmer. In the case of RAM to PLA mode of operation, the display includes the contents of the RAM as well as the contents of the PLA so that in a Manual mode it can be seen on a visual comparison basis that the terms have been programmed correctly. As each function has been completed, the response on the CRT indicates "Complete" and the change in message from one mode of operation to the other is also indicated. IF Not Verify occurs in any mode of operation, a "Fail" word will be indicated on the display of the CRT with the appropriate information contained in the device and RAM being displayed.

1.5 TERMS

New names are used on the PLA Programmer which are different from the standard Data I/O pROM Programmer. The new names which are used to define different sections of the PLA device unique to this Programmer are as follows:

1.5.1 PLA

"PLA" will be used generically throughout the Manual and means Programmable Logic Array. "FPLA" means Field Programmable Logic Array. Some manufacturers use "EPLA" while others use "FPLA" to indicate the electrically programmable species of PLA's. For simplicity, the term PLA will be used throughout.

1.5.2 PRODUCT TERM

The PLA contains 48 multi-input And Gates. Each one of these And Gates is called a Product Term. The Model $\overline{X}$ Programmer in its basic configuration will program up to 48 Product Terms which is the maximum number that the initial commercial PLA's contain. Referring to Figure 1, a typical PLA architecture is shown with the appropriate terms in their place. The And Gates are labeled Product Term and are indicated as No. Ø through 47.

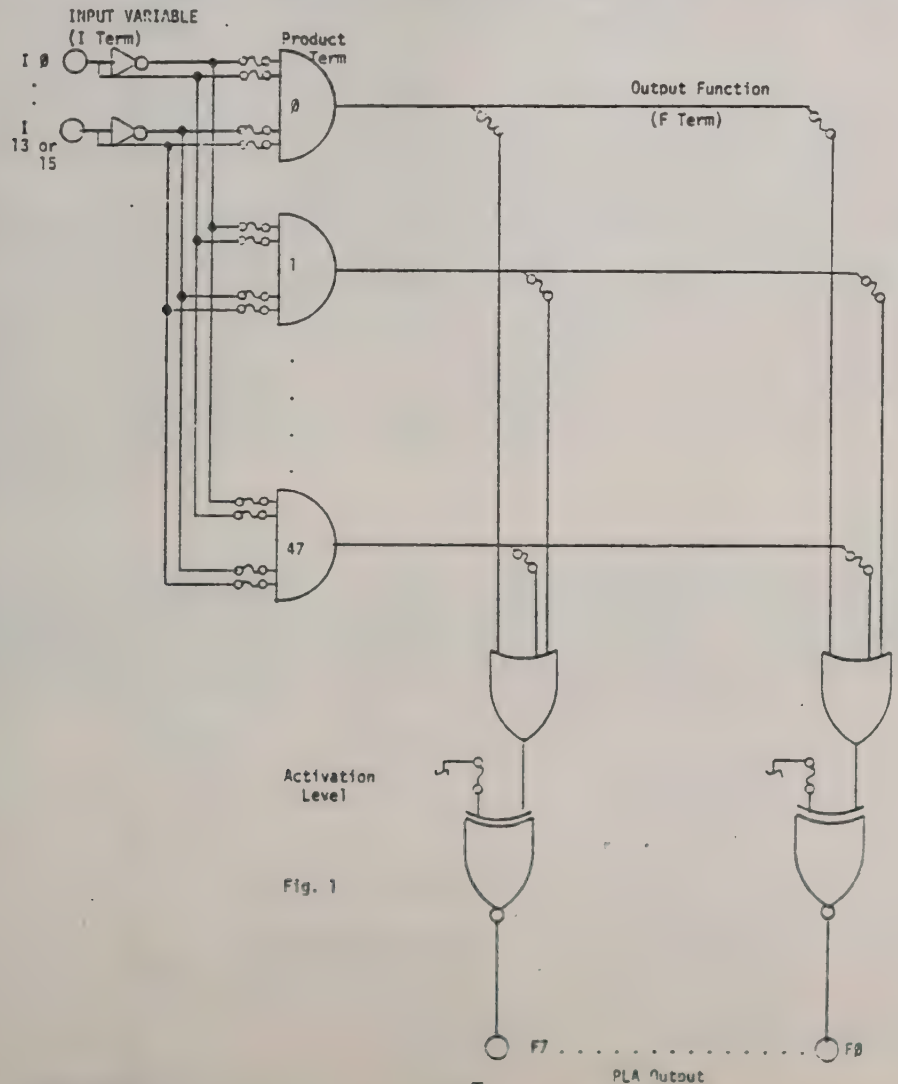


Fig. 1

1.5.3 I-Variable

The Input or I-Variable of the PLA are the 14 or 16 input variables that are programmed to allow a given Product Term to be responsive. These are the Input levels to the And Gates. Each I Variable associated with the pin number of the PLA contains both the true and complement (H or L) levels. For example, $I_{\emptyset}$ shown on Figure 1 is common to all Product Term Gates of the PLA (48) and has a programmable level associated with each Product Term in both the True and Complement form as is shown by the programmable elements of Product Term Ø. This Variable is programmable on all 48 Product Term levels separately so that the many inputs to a given Product Term may be altered for each Product Term to give total flexibility. The I-Variable may be programmed to -, L, H, or D. The D Key is inactive for Signetics PLA Programming. - = don't care, L= 1 var low, H= 1 var High, D= delete product term.

1.5.4 OUTPUT FUNCTION

The F-Term is the OR Output selected by each Product Term. Each Product Term may select any combination of the 8 output terminals of the PLA. This selection is made by programmable links at the outputs shown on Figure 1. Each of the 48 Product Term And Gates when it is selected may then form an 8-bit word to the Output terminals. The Output Function conditions are indicated on the CRT display panel as A (active) or - (inactive).

1.5.5 ACTIVE LEVEL

To complete the programmable variables of the PLA, the Output Activation Level is shown also in Figure 1 as the Exclusive-Nor component of the F-Terms This means that the Active Level may be asserted to a High Condition or Low Condition so that if an Active Level from a Product Term on a given level needs to be low, then the Activation Level for that Output Pin may be designated to that level prior to any other programming functions. The Activation level is programmed one time only and configures the PLA Output for all Product Terms. THE ACTIVE LEVEL IS ALWAYS ENTERED FIRST.

1.5.6 CURSOR

The Cursor is the pointer located on the CRT screen at which point data may be entered. It can be seen as an underscore in the character area which is used for data entry. The Cursor is used in the Keyboard to RAM mode of operation where the operator must place that pointer or Cursor to

the desired data entry location. Data may be changed pr altered in the Keyboard Mode by use of the Forward or Reverse Cursor keys (left or right arrow) to position the Cursor to the desired location. Appropriate data may then be intered in the position indicated by the Cursor.

2.0 OPERATING INSTRUCTIONS

The following operating instructions are detailed in a step-by-step procedure so as to inform the operator of the effects of each function control. Data Format is included in the operating instructions so that the Input Format may be strictly adhered to when preparing data from some external source.

2.1 KEYBOARD/RAM

This mode of operation is used to manually prepare data from the resident Keyboard on the front panel into the RAM Buffer. In order for this operation to properly occur, Program must also be selected so that data may be written in to the Ram Buffer. With this mode of operation selected, the entire Keyboard is active except CONTINUE. The Keys and their functions are described as follows;

2.1.1 ACTIVE LEVEL

Upon depressing Start in the Keyboard to Ram mode, the CRT Cursor will be allowing entry of ACTIVATION LEVEL. This requires that the operator enter H's or L's for the Active level consecutively until 8 entries have occured. If it is desired to skip the Active Level, the Forward key may be depressed to move the control system to the first or ØØ Product Term entry.

CRT DISPLAY

```
KEYBOARD TO RAM  ACTIVE
                   LEVEL
                 76543210
RAM LLLLHHHH
```

2.1.2 INPUT VARIABLE

The Input Variable is entered with - L H or D data keys being depressed for each entry consecutively. The Cursor will start at the most significant bit of the field and proceed toward the least significant bit. Corrections or deletions may occur by using the ⟵ or ⟶ keys on the keyboard to move the Cursor in either the left (backspace) or right (forward space)

```
PRODUCT    KEYBOARD TO RAM   ACTIVE
 TERM                          LEVEL
  ØØ                        76543210
                        RAM LLLLHHHH

      INPUT VARIABLE          OUTPUT
      1111                   FUNCTION
      321Ø9876543210         76543210
RAM   LLLLLLLLLL---L         -------A

                 PROGRAM
```

direction. The data which was displayed on the CRT will remain when moving the Cursor. However, when entering data, -, L, H, or D at a given Cursor position, the data which was stored in that location is updated and displayed at that time. As soon as the Input Term has been entered in its entirety, the Cursor automatically jumps to the Output Term for entry of A or - to represent Active or Inactive entry. The - and D keys are de-activated during the output entry.

2.1.3 Skipping Product Terms

Product Terms may be incremented or decremented by use of the Forward or Reverse key on the key pad. Each depression of the key shall move the Product Term counter forward by one and display the entire contents of the RAM on the CRT for visual indication. Depressing the Reverse key shall decrement the Product Term counter by one and redisplay the new content of the RAM for that Product Term address on the screen.

2.1.4 Clearing a Product Term

Depressing the Clear key on the key pad shall clear the contents of RAM for the given Product Term displayed, and the Cursor shall return to the most significant digit of the Input Term for data entry.

If the Clear Key is depressed, the entire Input and Output Term of that Product Term is cleared automatically, and the Cursor will return to the Input Variable MS

2.2 PLA-RAM

This mode of operation is used to enter (program) or verify the contents of the PLA with the RAM Buffer. A pre-programmed device is placed in the socket located on the right side of the control panel. When PLA-RAM and program are selected, only automatic selection is allowed with Auto causing the entire contents of the PLA to be written to RAM, and logically verified against the RAM.

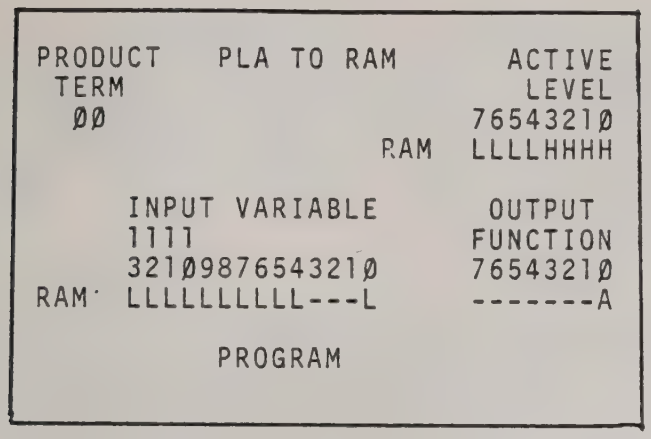
When it is desired to program the contents of the Master PLA into the RAM, Program must be selected prior to Start. If it is desired to Verify the contents of the RAM with the PLA, Verify must be selected prior to Start.

If an error occurs in verifying the contents of the PLA with the RAM, the machine will halt at the Product Term containing the verify error, with the word "fail" displayed at bottom of CRT. Continue may then be depressed to search for subsequent errors if desired. If Manual is selected, the machine will verify one Product Term at a time by use of the FWD and REV Product Term keys.

2.3 RAM CLEAR

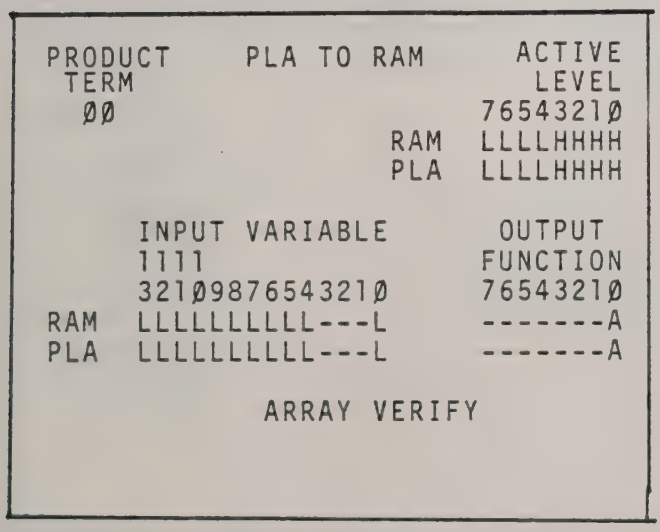
This mode of operation is used to automatically clear the RAM memory. It is often required to program less than 48 Product Terms; and in that case, RAM Clear is necessary to make sure that extraneous bits are not contained in the RAM when the Power is turned on or previous Product Terms which were contained in the RAM are completely erased. Depressing RAM Clear and Program, followed by Start shall cause the entire contents of RAM to be cleared. The state of the cleared RAM (either all - or all D or 0 and A) is dependent on the type of Personality Cards in the machine and the RAM Cleared state will match the states of the unprogrammed junctions of a virgin or new PLA.

CRT DISPLAY



Display shows PLA to RA
mode, Selected:
PROGRAM
AUTO
PLA/RAM
START

CRT DISPLAY



Display shows PLA to RA
mode, Selected:
ARRAY VERIFY
AUTO
PLA/RAM
START

A. Intersil

```
PRODUCT          RAM CLEAR          ACTIVE
 TERM                                LEVEL
  47                                7654321Ø
                                RAM LLLLLLLL

   INPUT VARIABLE                    OUTPUT
   1111                             FUNCTION
   321Ø9876543210                    7654321Ø

RAM-------------                     --------
```

B. Signetics

```
 PRODUCT          RAM CLEAR          ACTIVE
  TERM                                LEVEL
   47                                7654321Ø
                               RAM  HHHHHHHH

    INPUT VARIABLE                    OUTPUT
    111111                           FUNCTION
    54321Ø9876543210                  7654321Ø
RAM 0000000000000000                  AAAAAAAA
```

C. MMI

```
PRODUCT          RAM CLEAR          ACTIVE
 TERM                                LEVEL
  47                           RAM  7654321Ø
                                    HHHHHHHH

    INPUT VARIABLE                    OUTPUT
    1111                             FUNCTION
RAM 321Ø9876543210                    7654321Ø
    DDDDDDDDDDDDD                     AAAAAAAA
```

2.4 RAM TO PLA

This mode is used to Program or Verify the contents of RAM with the PLA. The mode selected allows any one of the four functions to be selected.

Each function is described individually as follows:

2.4.1 TEST NEW

Test New is a blank check effectively to determine if the PLA under test is, in fact, completely unprogrammed. To select Test New, RAM to PLA must be activated and Test New depressed. Depressing Start causes the system to test the PLA at high speed and any failure shall cause the display appropriately to say "Fail Test New." Continue may be depressed and machine will halt at next failure. If no failures occur, the word "complete" will appear at bottom of CRT display. No other operation shall occur following the Test New mode.

2.4.2 PROGRAM

In the Program mode of operation, prior to actual programming of any location a complete search of the PLA occurs to determine if any illegal bits occur in the device. An illegal bit is a programmable junction of the PLA which is already programmed, with the corresponding data in RAM in the unprogrammed state. This shall cause a Halt of the system with "Fail Illegal Bit Check" being displayed on the CRT.

In normal operation programming shall occur following the test for Illegal Bits. The Illegal Bits check may be omitted by removing JP2 of Logical Verify board.

As soon as Program has been successfully completed, the system automatically switches to the Array and Logical Verify sequence and passes through this sequence at extremely high speeds. The verify sequences may be omitted by removing JP1 on Logical Verify board.

All of the previous entries or sequences of operation occur when Program is selected on the function panel in the Automatic Mode of operation. Lesser modes of operation may be selected other than Program as desired by using the two verify keys.

2.4.3 LOGICAL VERIFY

Depressing the Logical Verify key in the Mode RAM to PLA illuminates that indicator and places the Programmer into the Logical Verify sequence of operation only. No test New or Program shall occur at this time. Depressing Start shall cause the display to indicate Logical Verify and the system will pass through the entire Logical Verify process and stop at the end indicating Complete. If an error occurs during the process of Logical Verify, Fail shall be indicated on the screen and if Manual is selected the concurrent Product Terms associated with the error will be displayed on the screen, along with the minterm input, the active level, PLA output, the synthesized RAM output, to give the operator an indication of what has transpired.

2.4.4 ARRAY VERIFY

Array Verify, when selected in the RAM to PLA mode of operation, places the Programmer into a mode of operation to compare the contents of the PLA with the RAM Buffer on a bit-by-bit basis. The total display is shown on the CRT screen of the contents of the RAM and the contents of the PLA. Automatic or Manual mode of operation may be selected. If Manual is selected, the system shall verify Product Term by Product Term by use of the FWD and REV Product Term keys on the front panel, with an error causing the word "Fail" to appear on the lower section of the screen. In the Automatic mode of operation, the

entire PLA shall be verified with the word Complete appearing at bottom of screen if the Array Verify is successful. If a failure occurs, the system shall halt with the word "Fail" appearing, showing the contents of RAM and PLA at the same time. Continue may be depressed and the machine will halt at the next failure.

2.5 POWER INTERRUPT

The Power Interrupt indicator is a blinking red lamp located in the center section of the key panel which is used to indicate that power has been interrupted or Start has not been depressed for the first time after Power ON has occurred. If, during normal operation, this indicator starts blinking, it assumes that the contents of the RAM have been lost and that re-programming must be necessary before programming a PLA to assure correctness of data.

CRT DISPLAY

```
PRODUCT     RAM TO PLA          ACTIVE
 TERM                             LEVEL
  ØØ                           76543210
                          RAM   LLLLHHHH
                          PLA   LLLLHHHH

      INPUT VARIABLE          OUTPUT
      1111                    FUNCTION
      3210987654321Ø          76543210
RAM   LLLLLLLLLL---L          -------A
PLA   LLLLLLLLLL---L          -------A

              Illegal Bit Check
```

Display shows testing for Illegal Bits which occurs prior to Programming. Can be omitted by removing jumper JP2 on Log. Ver. board.

CRT DISPLAY

```
PRODUCT     RAM TO PLA          ACTIVE
 TERM                             LEVEL
  ØØ                           76543210
                          RAM   LLLLHHHH
                          PLA   LLLLHHHH

      INPUT VARIABLE          OUTPUT
      1111                    FUNCTION
      3210987654321Ø          76543210
RAM   LLLLLLLLLL---L          -------A
PLA   LLLLLLLLLL---L          -------A

                PROGRAM
```

As programming progresses Ram and PLA match.

CRT display for array verify is identical to display for array verify in PLA-RAM mode.

CRT DISPLAY

LOGICAL VERIFY MANUAL DISPLAY (FAILURE)

```
                RAM TO PLA    OUTPUT
 MINTERM INPUT                76543210
 111111                   ACT LLLLHHHH
 543210987654321Ø         RAM HHHHHLLL
 LLLLHHHHLLLLHHHH         PLA HHHHHLHL

          CONCURRENT PRODUCT TERMS
 00   01   02   03   04   05   06   07
 08   09   10   11   12   13   14   15
 16   17   18   19   20   21   22   23
 24   25   26   27   28   29   30   31
 32   33   34   35   36   37   38   39
 40   41   42   43   44   45   46   47

                 FAIL
            LOGICAL VERIFY
          CONTINUE IF DESIRED
```

INTRODUCTION FORMATS

The following sections describe the Input and Translatable Formats of the Model X system. Careful attention to detail of this section is necessary for error free preparation of data.

2.6 INPUT/RAM

This mode is used to copy the contents of the Input Device to the RAM Buffer. The Input Format must be strictly adhered to for entering data into the RAM Buffer from any input source, including Mark Sense Card Reader, Punched Paper Tape, or Remote Input - either serial or parallel. The Input Format is shown below for both Mark Sense Card and Punched Paper Tape. Display example on next 2 pages.

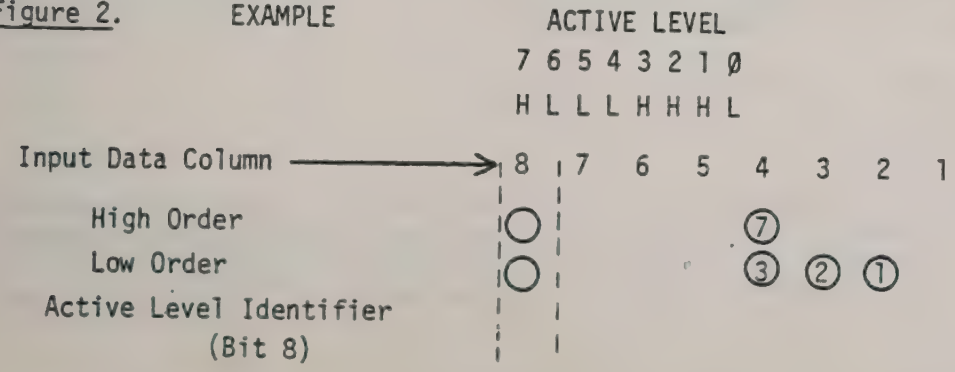
2.6.1 INPUT FORMAT

With the Input/RAM mode selected for operation, machine coded data must be used for data entry into the Programmer. The following is a sequential list of instructions which must occur to successfully enter information into the RAM.

2.6.2 ACTIVE LEVEL

The Active Level must first be entered prior to any other data on the Input Tape. The Active Level is detected in the Programmer with a Bit 8 and the Low Order bits of 1 through 4. (See Figure 2.) The Bit 8 detects the data as Input Active Level information. The High order word must be entered first (7 through 4) followed by the Low order (3 through Ø). To properly enter the Active Level, a mark on a card or punched hole on paper tape represents an H or High as an Active Level with a no punch or no mark equaling an L for a Low Active Level. The example below shows the Active level entry for an Active Level HLLLHHHL. This means that the first Active Level entry (High Order) contains a hole in bits 8 and 4, so that bit 8 detects Active Level and bit 4 places the H in the 7 position with 3, 2, and 1 channels representing an L for 6, 5, and 4 positions of the Active Level Entry.

Figure 2. EXAMPLE



The Low Order entry or second character uses the 8 bit to detect Active Level once again, and the holes in channels 4, 3, and 2 to represent H Level entries for bits 3, 2, and 1 of the display. A no hole in position 1 of the Low order entry allows the L to be entered into the Ø position of the Active Level entry display.

2.6.3 PRODUCT TERM NUMBER

The Product Term Number must be entered prior to I-Variable and F-Data so that the Programmer will know which entry sector in RAM that the data is being routed. The Product Term Number need not be sequential, since the number is commanded on the Punched Paper Tape or Input Mark Sense Card as the routing or preset number into the RAM for the Product Term Address. The most significant digit is presented first, followed by the least significant digit in BCD Format. Referring to Figure 3, it can be seen that to enter the Product Term Number 15, the Bit level assignment on Input MSCR or Paper Tape assumes a BCD Power of 8, 4, 2, 1, on Channels 4, 3, 2, and 1 respectively.

Figure 3. PRODUCT TERM NUMBER

1. Enter most significant digit first
2. BCD Format

   To enter Product Term 15, enter 1, then 5
3. Bit 7 allows entry of Product Term.

					(8	4	2	1) BCD Power
Input Data Column ⟶	8	7	6	5	4	3	2	1	
MSD P/T		⑦						①	1
LSD P/T		⑦				③		①	5

Product Term Number Identifier (Bit 7)

Note: Entering Bit 5 in both rows along with P/T number causes skip of Product Term entry.

The most significant digit product term entry includes a bit 7 to cue Product Term entry along with Bit 1 for the most significant digit one. The least significant digit Product Term entry includes a bit 7 followed by a 1 and 3 bit for BCD 5.

The maximum Product Term entry permissible is 47.

2.6.4 INPUT VARIABLE

Entry of the Input Variable is detected with bits 7 and 8 being present simultaneously. For the proper entry of Input Variables, 7 words must be used for entering the Input Variables for Intersil FPLA's (14 Input) and 8 words must be used for entering Input Variables for Signetics (16 input) FLPA.

The most significant bit of the Input Variable is presented first with the least significant bit being entered last. Two Input Variable components are entered on each Input Variable Line in actual machine coded format. The two entries represent a -, L, H, or D coding for each line assignment 13 through Ø or 15 through Ø. Referring to Figure 4, the coding assignments for the Input Variables are shown. Bit 7 and 8 are always used to introduce the Input Variable Code with the first character representing the highest order bit assignment (in this instance 13 followed by 12).

The High Order 13 is located on bits 3 and 4 of the Input Data word and the coding for the two lines are 13 and $\overline{13}$ for positions 4 and 3 respectively. In the center of the figure are the four line assignments -, L, H, and D with - representing no hole in either the true or complement entry. L represents a hole in the complement entry ($\overline{13}$). An H represents a hole in the true entry (13) and a D represents a hole in both entries (13 and $\overline{13}$).

This must be accomplished for each level entry word so that if the first 4 entires of the Input Variables 13, 12, 11 and 10 are to be entered -, L, H, and D as is shown in the Figure, the two punched paper tape words to represent those entries would be shown as follows: The 8 and 7 would represent the Input with a hole in position 2 of that word to represent the H or 12. No holes in 3 and 4 would represent a - in level 13. The second character with the 8 and 7 again introduces Input Term with a hole in 3 representing an L for the 11 entry and 1 and 2 to represent a delete or D for position 10. The same procedure is followed on down through bit position Ø.

Figure 4.

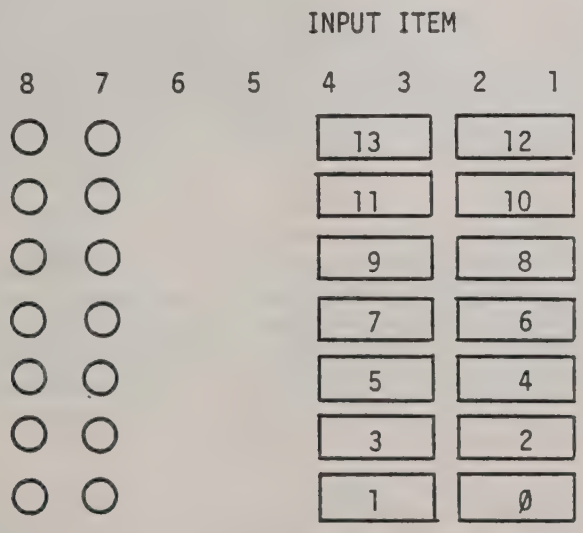
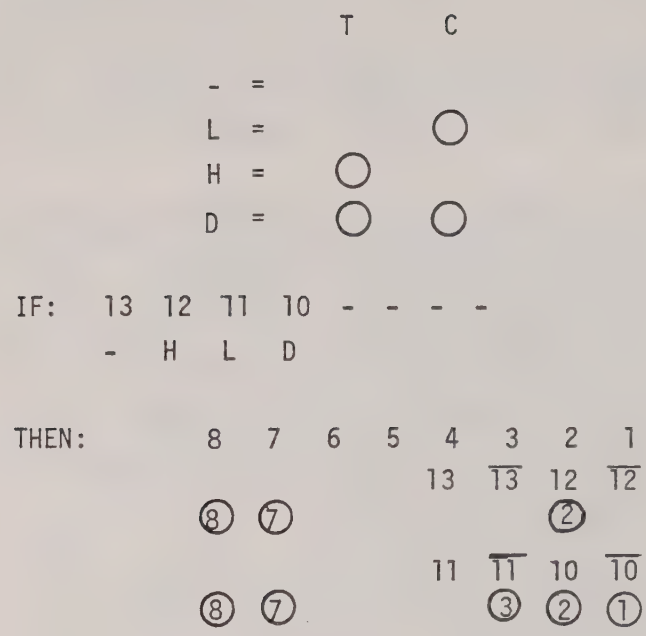


Figure 4 continued on the next page.

Figure 4 continued



2.6.5 OUTPUT FUNCTION

The Output Function or F Term is cued on the coding of Punched Paper Tape or Ma Sense Cards by a bit or hole in position 6 with the most significant bits 7, 6, 5, and 4 occurring on the channels 4, 3, 2 and 1 of the Punched Paper Tape or Mark Sense Card and the second line entry to also include a bit 6 with the least significant entry 3, 2, 1 and Ø on channels 4, 3, 2, and 1 respectively. Figure 5 shows the two entries for the output data. A hole in the respective position represents an Active Output and a no hole represents an in-active Ouput. The example shown provides an Active Term of 7, 6, 4, and 1 which allows the Punched Paper Tape coding (or Mark Sense Card Reader coding) to present the Output Function in two words with the most significant bits first, followed by the least significant bits. A hole in channel 6, 4, 3 and 1 represents the High Order Word introducing the Output Function with bit 6 and the 7,6 and 4 Active Level in Channels 4, 3 and 1. The second character contains a bit 6 to represent Output Function and a hole in Channel 1 to activate bit 1 of the Output Function.

Figure 5 OUTPUT TERM

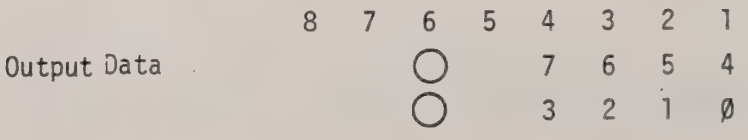


Figure 5 Continued

EXAMPLE

If Output Function=	7	6	5	4	3	2	1	Ø
	A	A	-	A	-	-	A	-

Then Paper Tape coding would be:

8	7	6	5	4	3	2	1
		○		⑦	⑥		④
		○				①	

The composite coding of an Input Entry is shown on Figure 6. It is noted that the first entry is the activation level followed by Product Term number, Input Variables and Output Function. From that point forward, the Product Term number, Input Variables and Output Function are repeated with the respective data assigned. After the last entry occurs, the end of Text code must be entered on the Punched Paper Tape which is detected with a Bit 8, 7, and 6 occurring simultaneously. This will cause a system stop with the word "COMPLETE" being displayed on the CRT.

It may be desired to enter a single product term into the RAM from the Input source. This may be to change an entry from an existing entry or to program a single entry into a PLA device. The same procedure must be used as previously described, entering the active level along with the Product Term number, the Input Variable, the Output Function and if only one entry is used, End of Text is entered to terminate entry.

2.7 TRANSLATOR/RAM

The Translator/RAM Mode of operation is used to input data to the FPLA Programmer from either the resident Punch Tape Reader or Remote Parallel Input Interface, in formatted ASCII coded information. The translatable format is compatible with the manufacturers published format shown on page ~~17~~ 25 (figure 7). Display examples are shown on the following 2 pages.

2.7.1 STX

The STX character (Start of Text) is used to initiate or start translation. Header information or identifying visual characters may be placed on the tape or input data stream prior to the start of conversion for identifying records as being necessary by the particular customers data preparation needs. The character STX, however, signals to the translator that the Start of translation is now taking place and therefore, activate the translator and the program format in the Model X for translation. STX is coded as a Hex Ø1 or Ø2 (Control A or B on teletype).

2.7.2 ACTIVATION LEVEL

The Activation Level is entered on the translation format (refer to figure 7) by prefixing the Active Level field with the control characters Asterick A.

CRT DISPLAY

```
PRODUCT  INPUT TO RAM      ACTIVE
 TERM                       LEVEL
  ØØ                      76543210
                     RAM  LLLLHHHH
                     PLA  LLLLHHHH

      INPUT VARIABLE       OUTPUT
      1111                 FUNCTION
      3210987654321Ø       76543210
RAM   LLLLLLLLLL---L       ********A
          LLLLLL---L       ********A

              PROGRAM
```

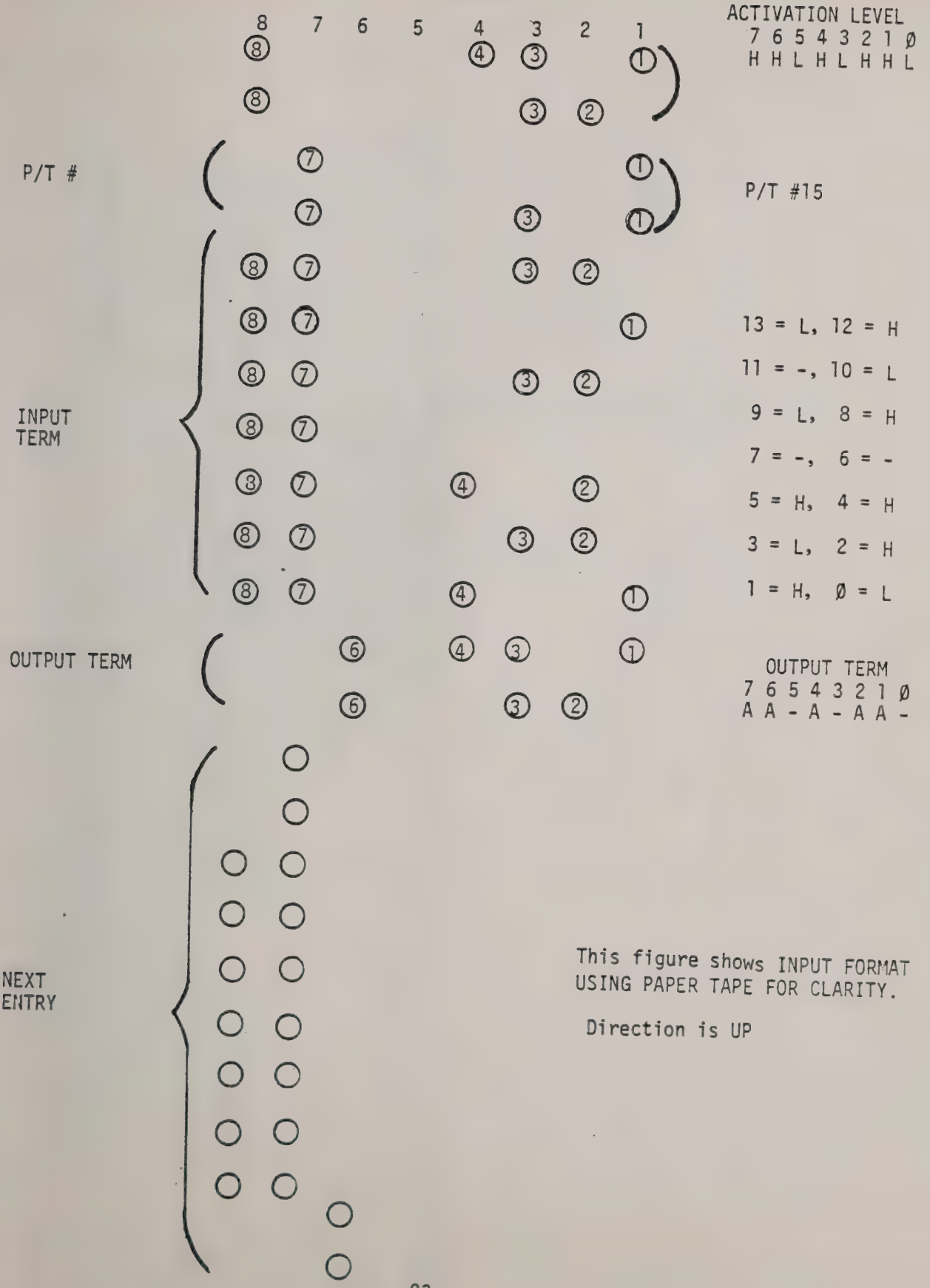
CRT DISPLAY

```
PRODUCT   INPUT TO RAM       ACTIVE
 TERM                         LEVEL
  ØØ                        76543210
                      RAM   LLLLHHHH
                      EXT   LLLLHHHH

     INPUT VARIABLE          OUTPUT
     1111                    FUNCTION
     3210987654321Ø          76543210
RAM  LLLLLLLLLL---L          --------A
EXT  LLLLLLLLLL---L          --------A

           ARRAY VERIFY
```

Figure 6


8 7 6 5 4 3 2 1
ACTIVATION LEVEL
7 6 5 4 3 2 1 Ø
H H L H L H H L
P/T #
P/T #15
INPUT TERM
13 = L, 12 = H
11 = -, 10 = L
9 = L, 8 = H
7 = -, 6 = -
5 = H, 4 = H
3 = L, 2 = H
1 = H, Ø = L
OUTPUT TERM
OUTPUT TERM
7 6 5 4 3 2 1 Ø
A A - A - A A -
NEXT ENTRY

This figure shows INPUT FORMAT USING PAPER TAPE FOR CLARITY.

Direction is UP

CRT DISPLAY

```
PRODUCT    TRANSLATE TO RAM    ACTIVE
 TERM                           LEVEL
  ØØ                          76543210
                        RAM   LLLLHHHH

      INPUT VARIABLE          OUTPUT
      1111                    FUNCTION
      3210987654321Ø          7654321Ø
RAM   LLLLLLLLLL---L          -------A

              PROGRAM
```

CRT DISPLAY

```
PRODUCT    TRANSLATE TO RAM    ACTIVE
 TERM                           LEVEL
  ØØ                          76543210
                        RAM   LLLLHHHH
                        EXT   LLLLHHHH

      INPUT VARIABLE          OUTPUT
      1111                    FUNCTION
      3210987654321Ø          7654321Ø
RAM   LLLLLLLLLL---L          -------A
EXT   LLLLLLLLLL---L          -------A

          ARRAY VERIFY
```

Figure 7

```
STX                          *A LLLLLLLL

*P ØØ *I LL---L--------H *F ••••••AA•
*P Ø1 *I LLLLLL-------- *F A••••AAA
*P Ø2 *I HLLLLH-------- *F AA•••AA•
*P Ø3 *I HHLLLH-------- *F -A---A--
*P Ø4 *I LHLLLH------H- *F --A--AA-
*P Ø5 *I LHLLLH-----HL- *F ---A-AA-
*P Ø6 *I LHLLLH----HLL- *F --AA-AA-
*P Ø7 *I LHLLLH---HLLL- *F ----AAA-
*P Ø8 *I LHLLLH--HLLLL- *F --A-AAA-
*P Ø9 *I LHLLLH-HLLLLL- *F ---AAAA-
*P 1Ø *I LHLLLHHLLLLLL- *F --AAAAA-
*P 11 *I LHLLLHLLLLLLL- *F A-----AA
*P 12 *I LL---L------HL *F --A--AA-
*P 13 *I LLHLLH----H--- *F A-A--AAA
*P 14 *I HLHLLH-------- *F AAA--AA-
*P 15 *I HHHLLH-----H-- *F -AA--A--
*P 16 *I LHHLLH-----H-- *F ---A-AA-
*P 17 *I LHHLLH----HL-- *F --AA-AA-
*P 18 *I LHHLLH---HLL-- *F ----AAA-
*P 19 *I LHHLLH--HLLL-- *F --A-AAA-
*P 2Ø *I LHHLLH-HLLLL-- *F ---AAAA-
*P 21 *I LHHLLHHLLLLL-- *F --AAAAA-
*P 22 *I LHHLLHLLLLLL-H *F -----AA-
*P 23 *I LHHLLHLLLLLL-L *F -A----A-
*P 24 *I LL---L-----HLL *F ---A-AA-
*P 25 *I LLLHLH-------- *F A--A-AAA
*P 26 *I HLLHLH-----L-- *F AA-A-AA-
*P 27 *I HHLHLH-------- *F -A-A-A--
*P 28 *I LHLHLH----H--- *F --AA-AA-
*P 29 *I LHLHLH---HL--- *F ----AAA-
*P 3Ø *I LHLHLH--HLL-L- *F --A-AAA-
*P 31 *I LHLHLH-HLLL--- *F ---AAAA-
*P 32 *I LHLHLHHLLLL--- *F --AAAAA-
*P 33 *I LHLHLHLLLLL--H *F -----AA-
*P 34 *I LHLHLHLLLLL-HL *F --A--AA-
*P 35 *I LHLHLHLLLLL-LL *F -A----A-
*P 36 *I LL---L----HLLL *F --AA-AA-
*P 37 *I LLHHLH-------- *F A-AA-AAA
*P 38 *I HLHHLH-----L-- *F AAAA-AA-
*P 39 *I HHHHLH-------- *F -AAA-A--
*P 4Ø *I LHHHLH---H---- *F ----AAA-
*P 41 *I LHHHLH--HL--L- *F --A-AAA-
*P 42 *I LHHHLH-HLL---- *F ---AAAA-
*P 43 *I LHHHLHHLLL-H-- *F --AAAAA-
*P 44 *I LHHHLHLLLL---H *F -----AA-
*P 45 *I LHHHLHLLLL--HL *F --A--AA-
*P 46 *I LHHHLHLLLL--LL *F ---A-AA-
*P 47 *I LHHHLHLLLL-LLL *F •••••••••

                             ETX
```

TRANSLATING INPUT FORMAT

These two sequential words inform the translator that the following word sequence is the Activation Level desired in the programming format.

Asterisk A and the Activation Level may be entered only once in the entire translation sequence.

2.7.3 PRODUCT TERM

The Product Term entry follows the entry of the Activation Level as it is shown on Figure 7. To introduce a Product Term, Asterisk P space is used as the identifier sequence. The following characters are ASCII coded decimal numbers to designate the Product Term number for routing the Input and F Term information. Note that there must be one space between the asterisk P and the two digit Product Term number.

2.7.4 INPUT TERM

The Input Term is identified with an Asterisk I. Following this identifier, 14 (Intersil) or 16 (Signetics) entries must be made into the data field (H, L, -, or D). The most significant bit (I_{13} or I_{15}) is presented first and then proceeding to the least significant bit ($I_{\emptyset}$)

2.7.5 F TERM (Output Function)

The F Term data field associated with the Product Term number defined is presented following the I or Input Term. To identify the Output Function Asterisk F is used for the prefix decoder. The following 8 ASCII words shall be - or . for inactive and A for active. No other words may be entered in this field.

The data fields repeat in the same process previously described to a maximum of forth-eight Product Term Entries. The Product Term entires may or may not be desired to be in order, and if they are not, the proper information is routed into the machine as identified by the Asterisk P space and Product Term number.

2.7.6 ERROR FIELDS

If it is desired during the preparation of information to erase or cancel a given Product Term entry, this may be done by first entering Asterisk P, space, the Product Term number desired to be erased, followed by the Character E. The E character may occur only immediately following the two digit Product Term number. This will cause data in the indicated Product Term to be cleared in RAM. In addition, if an error is made in preparing a tape on a teletype machine such that an incorrect character is punched inside a data field, then a backspace and rubout may be used by the teletype operator to make the correction. The machine will ignore the rubout and interpret the correct data characters as if the rubout were not present. Also note that if an entry is made twice for the same Product Term number, the last entry the machine reads will be written into RAM.

7.7 ETX

Any number of entries may be presented through the coded translator input format. As the desired number of entries have been entered, the end of test (ETX) character is entered to stop translation. ETX is coded as a Hexidecimal 03 (Control C) which causes translation to cease.

7.8 CAUTION NOTE

The above described translate format must be strictly adhered to. However, to facilitate an easily readable printout of a translate coded paper tape, spaces, carriage returns, and line feeds may be intersperced before and after the identifiers (*A, *I, *F) with one exception. There must be exactly one space between the *P and the two digit product number. All other spaces are optional.

2.8

SIGNETICS FPLA

PROGRAM PULSE MONITORING PROCEDURE

I. MONITOR ACTIVE LEVEL PROGRAMMING WAVEFORMS

A) Fit Socket Assembly with 150 Ohm resistors to ground on all eight output pins of socket (Pins 10-13 and 15-18).

B) Select PLA to RAM, Program, Automatic and load the RAM.

C) Select the Keyboard to RAM mode and enter an L in an Active Level Location.

D) Select RAM to PLA, Program, Automatic. Hit Reset and depress Start. The various programming waveforms can be observed and compared to the timing diagram.

II. MONITOR INPUT VARIABLE PROGRAMMING WAVEFORMS

A) Perform steps A and B of I

B) Select the Keyboard to RAM Mode. Enter a -, H, or L in a desired Product Term and Input Variable location.

C) Perform Step D of I to observe the various waveforms.

III. MONITOR OUTPUT VARIABLE PROGRAMMING WAVEFORMS

A) Perform steps A and B of I.

B) Select the Keyboard to RAM mode. Enter L in all eight Active Level locations. Enter all A's in the Output Variable locations of the first few Product Terms. Enter a period in an Output Variable location of one of these Product Terms.

C) Select RAM to PLA, Program, Manual. Hit Reset and depress Start. The Programmer will perform Illegal Bit Check and Halt. Depress Enter. The Programmer will be trying to program the Active Levels. Temporarily disconnect the 8 150 Ohm resistors from ground. Reconnect the resistors and depress Enter until the Product Term with the Bit to Program in the Output Variable location is reached. The various waveforms can now be observed.

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

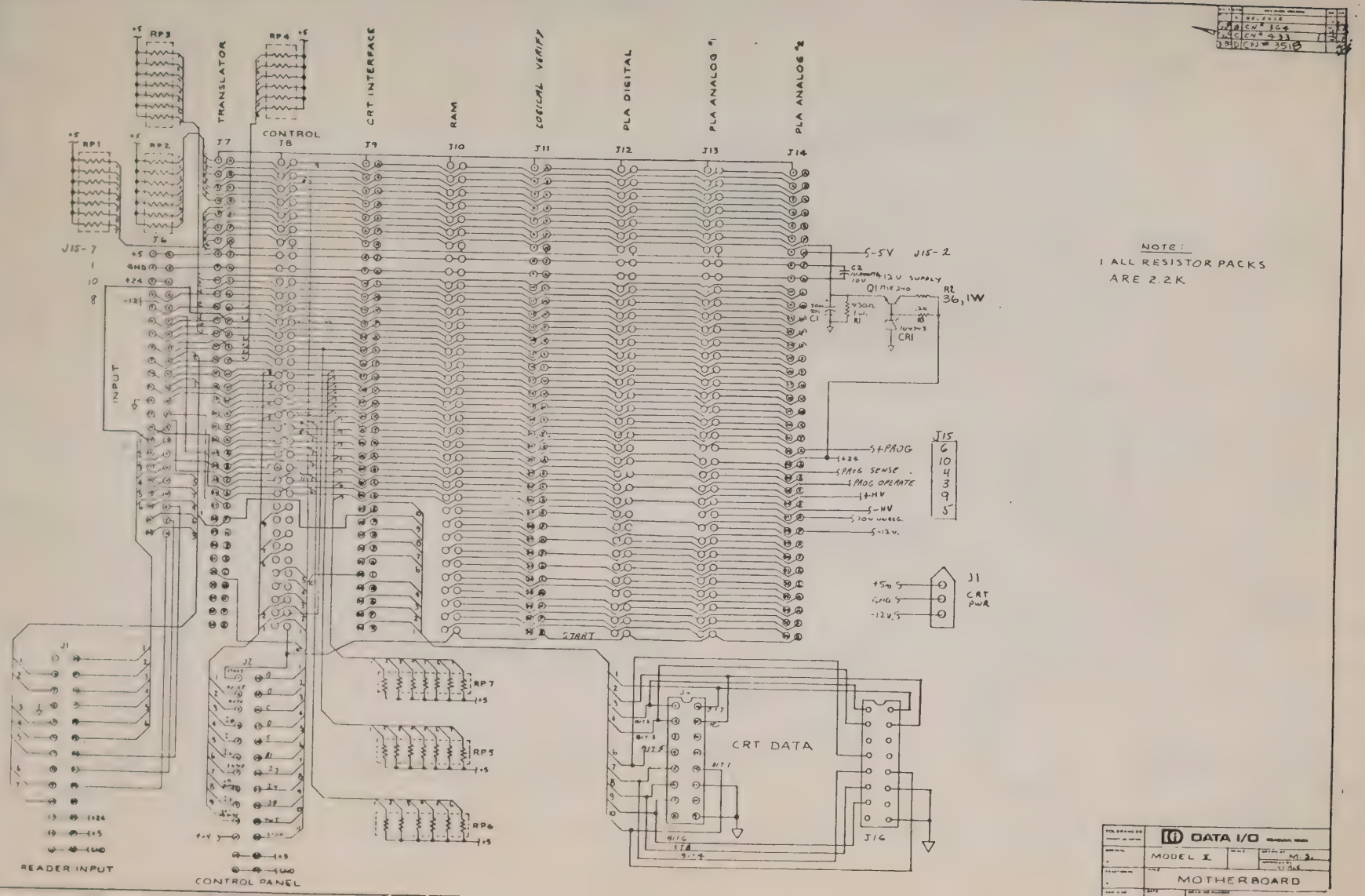
Please send all parts orders to:

DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

From Europe:

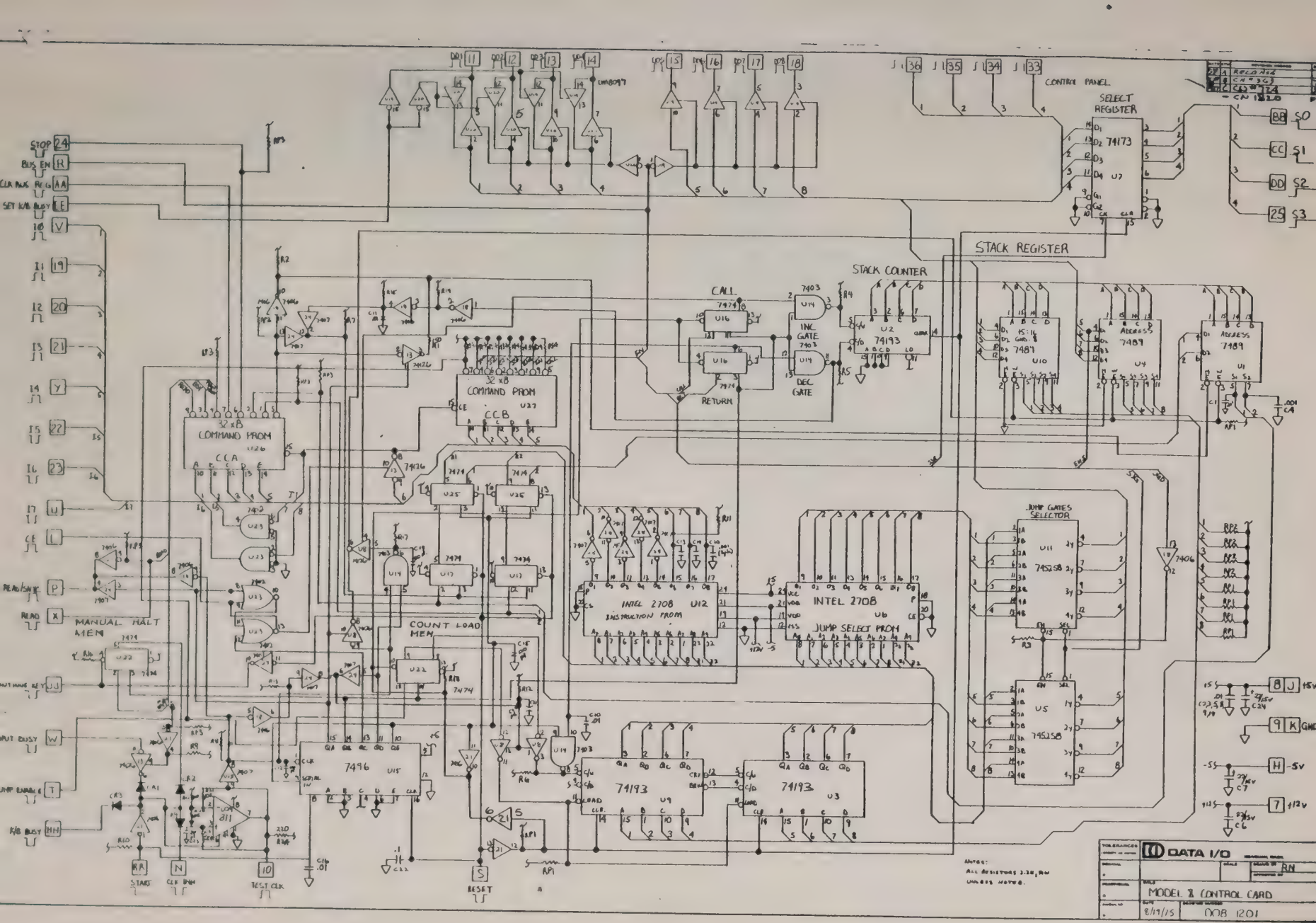
DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

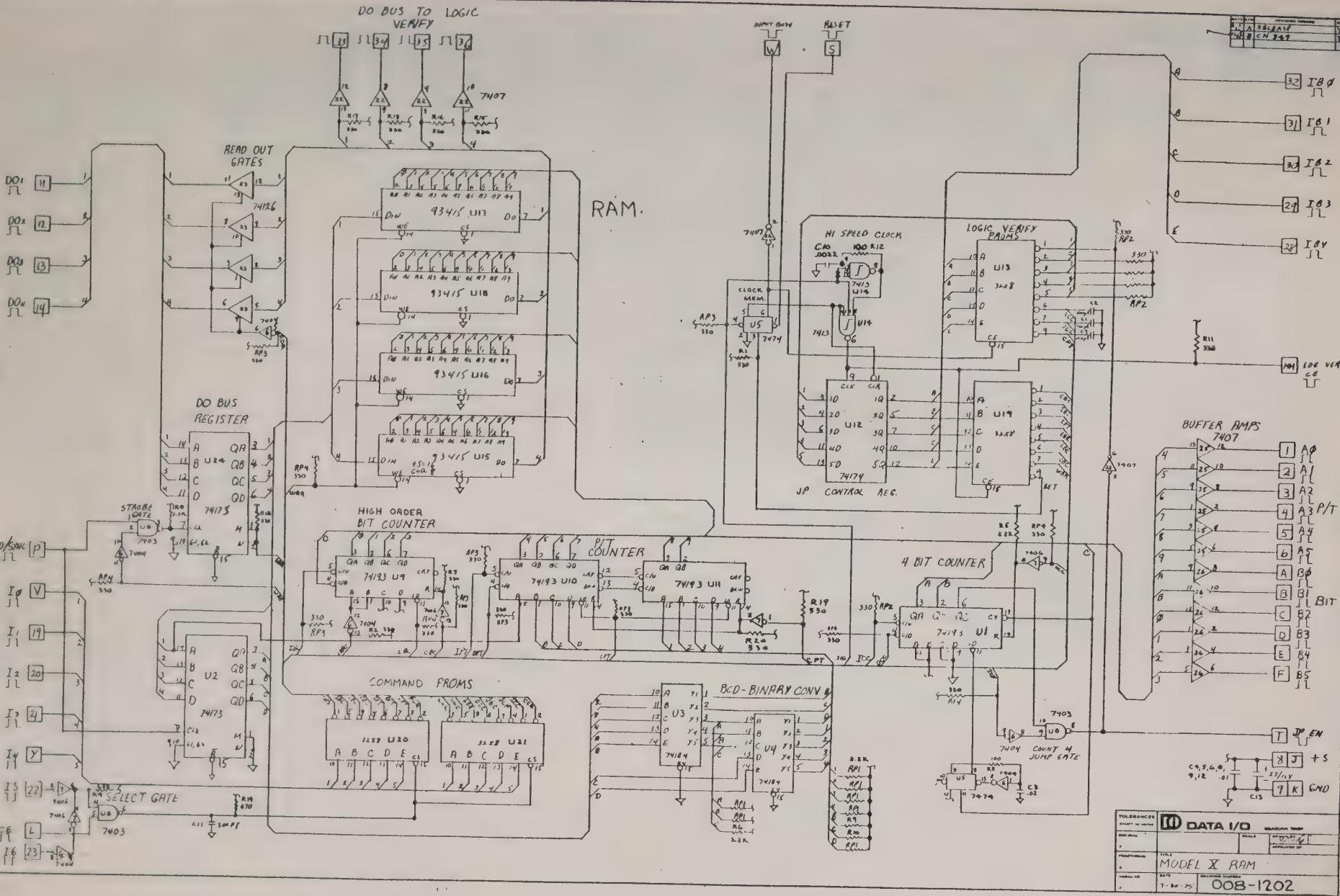
8
7
6
5
4
3
2
1
D
C
B
A
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B CN 008 7-8-74 MZ
C CN 007 7-15-74 MZ
D CN 020 7-25-74 MZ
E CN 021 7-28-74 MZ
F CN 025 8-8-74 MZ
G CN 037 10-11-74 MZ
H CN 082 12-19-74 MZ
J CN 152 3-11-75 MZ
K CN 183 4-30-75 MZ
L CN 461 2-11-76 MZ
M CN 479 2-17-76 MZ
N CN 532A 3-15-76 MZ
P CN # 712 8-26-76
R CN # 775 10-20-76
S CN # 1710 8-30-77
J1 PIN MOLEX
J2 12 PIN MOLEX
JP1 TEST NORM.
F3
MDA 970-1 D1
MDA 960-3 D2
MDA 960-3 D4
MDA 960-3 D3
C13 10,000 16V
C14 1000MF 25V
C15 1000MF 75V
C16 2300MF 50V
C17 30MF 75V
C18 4.7 MF, 50V
C1 4.7MF 35V
C2 4.7MF 35V
C3 50MF 50V
C4 50MF 50V
C5 50MF 75V
C6 .001
C7 47MF 6V
C8 OMIT
C9 .01
C10 .001
C11 .001
U1 723
U2 723
U3 723
U4 723
U5 723
Q1 MJ3000
Q2 TIP 32A
Q3 TIP 32A
Q4 2N2484
Q5 2N2484
Q6 TIP 36C
Q7 TIP 38A
Q8 TIP 38A
Q9 MJE 240
Q11 2N2907A
Q12 2N2484
Q13 2N2484
CR1 IN4734
CR2 IN4749
CR3 IN4001
CR4 IN4001
CR5 IN4755
CR6 IN4754
CR7 IN4148
CR8 IN4148
CR9 IN4753
CR10 IN751
CR11 IN4736A
CR12 IN4735A
CR13 IN4148
CR14 IN4148
CR15 IN4148
CR16 IN4148
F2 .5A FAST BLOW
R1 4.99K, 1%
R2 6.04K 1%
R3 11K, 1%
R4 .33, 1W, 5%
R5 100 1W
R6 10K 1%
R10 9.1K
R11 .05 2W 5%
R12 100K
R13 330, 1W
R14 33.6% 1W
R15 4.7K
R16 1K
R17 2K
R18 10K 10TURN
R19 1K
R20 2.4K 1W
R21 4.7K
R22 8.1K
R23 10K
R24 10K 10 TURN
R25 1.2K
R26 1K 10 TURN
R27 9K
R28 2K
R29 9.1K
R30 1K
R31 .51, 5%
R32 47K
R33 47K
R34 470
R35 2.2K
R36 430, 1W
R37 4.7K
R38 47K
R39 .5, 1W 5%
R40 10K 10 TURN
R41 47K
R42 2.4K 1W
R43 47K
R44 47K
R45 1K
R46 2K
R47 2K
R48 8K
R49 1K
R50 10K
R51 10K
R52 2.2K
R53 750
R54 2.4K
R55 2.2K
R56 2.2K
R57 2.2K
R58 47K
R59 10K
+5V B 5A
GND A
M
-5V B .25A
-12V H .5A
+24V K 1.5A
+PROG. F .5A
SENSE D
OPERATE C
UNREG. HV L
+HV J
-HV E
POWER SUPPLY TO MEU
J2 MEU MODELS 80 90 MEU MODELS 385 SIGNAL
1 E4 E4 GND
2 E6 E6 -5
3 E12 E12 PROG OPR
4 E11 E11 PROG SENS
5 E8 E8 -HV
6 E1 E1 +PROG
7 E3 E3 +5
8 E2 E2 -9
9 E10 E10 +HV
10 E5 E5 +24
11 E9 E9 UNREG HV
12 E7 E7 GND
DATA I/O
POWER SUPPLY
DRAWN: G. NIEBEL
APVD:
SIZE D
CODE IDENT NO 54193
DRAWING NO 008-1087
SCALE
SHEET

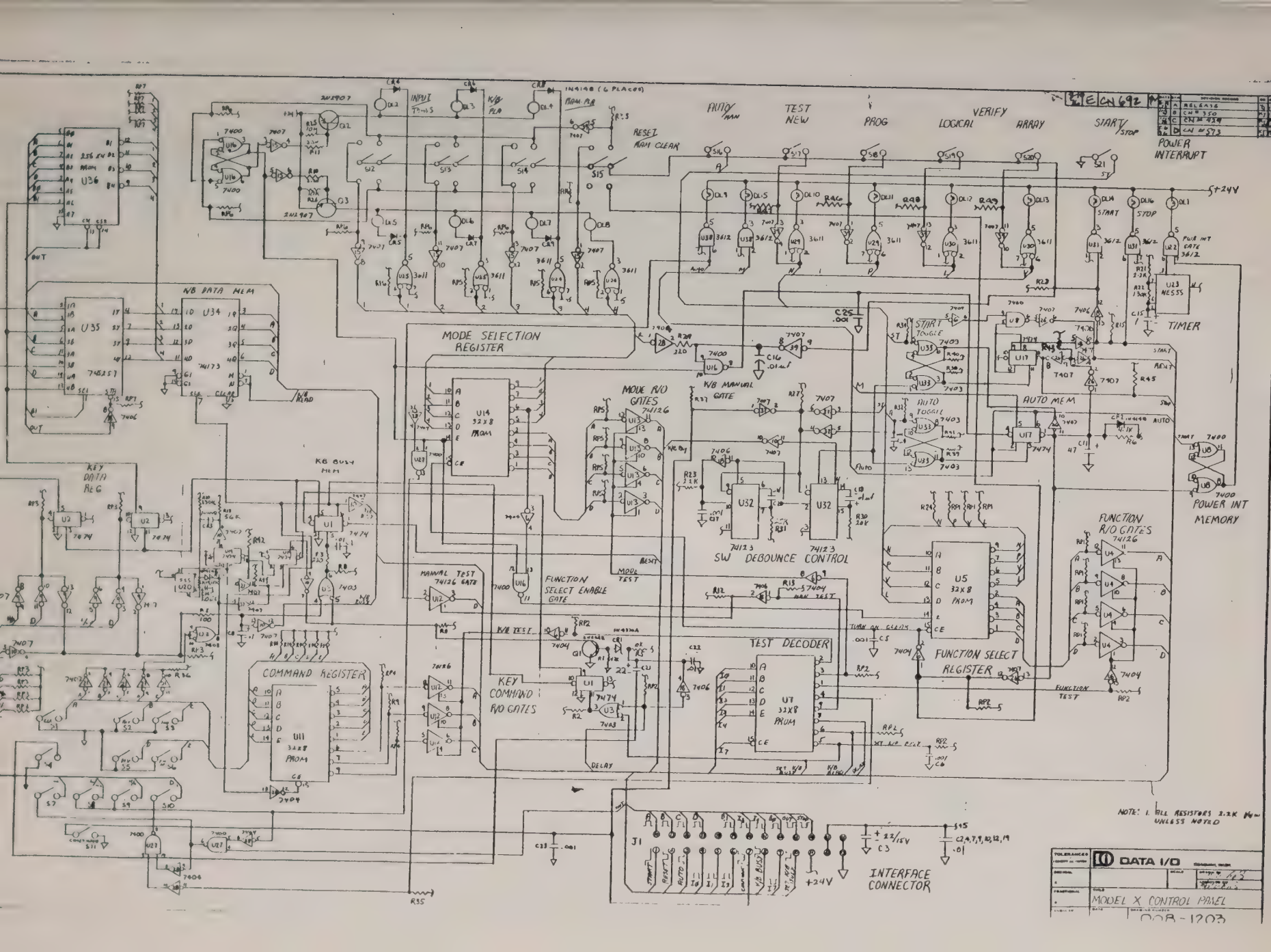


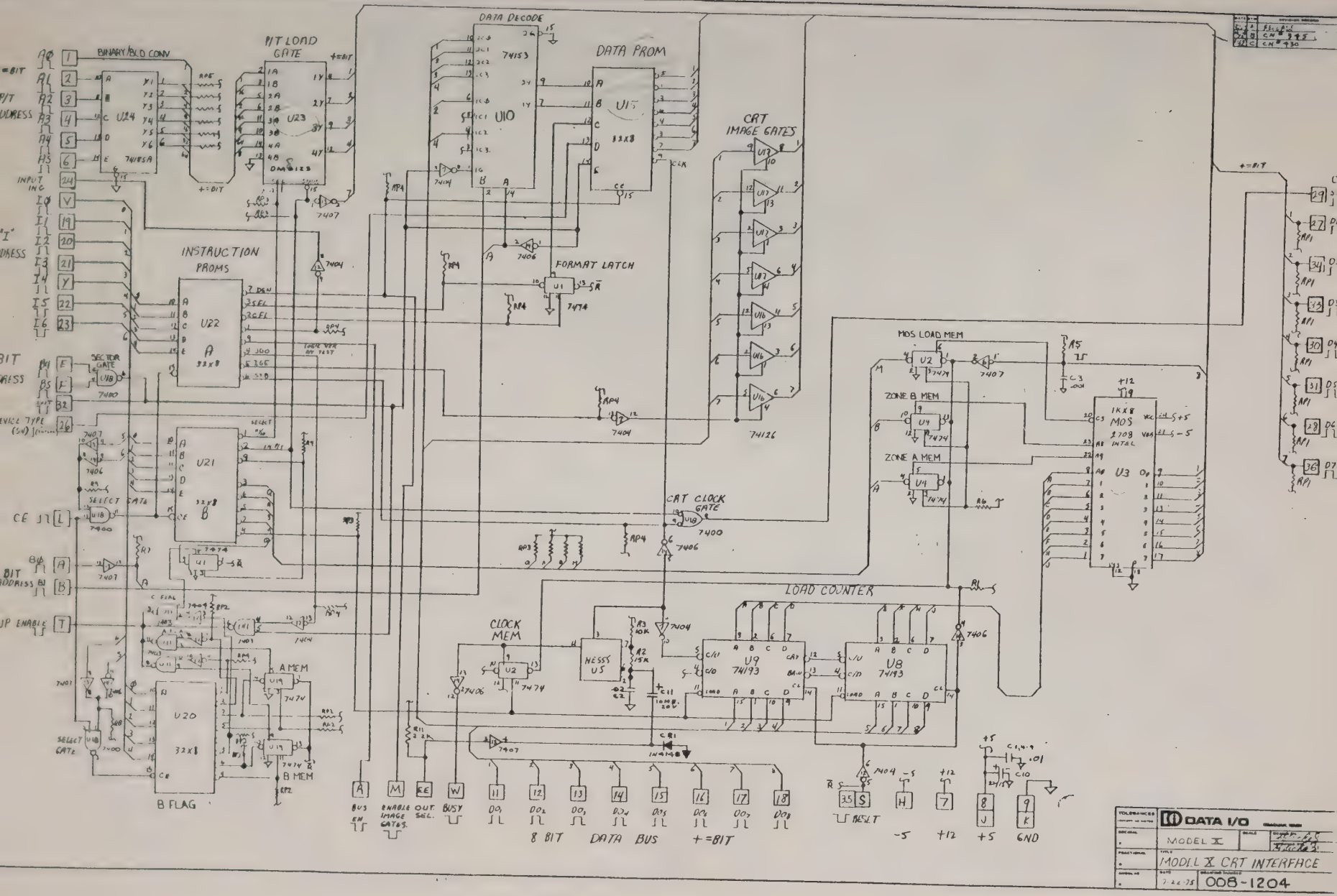
NOTE:
1 ALL RESISTOR PACKS ARE 2.2K

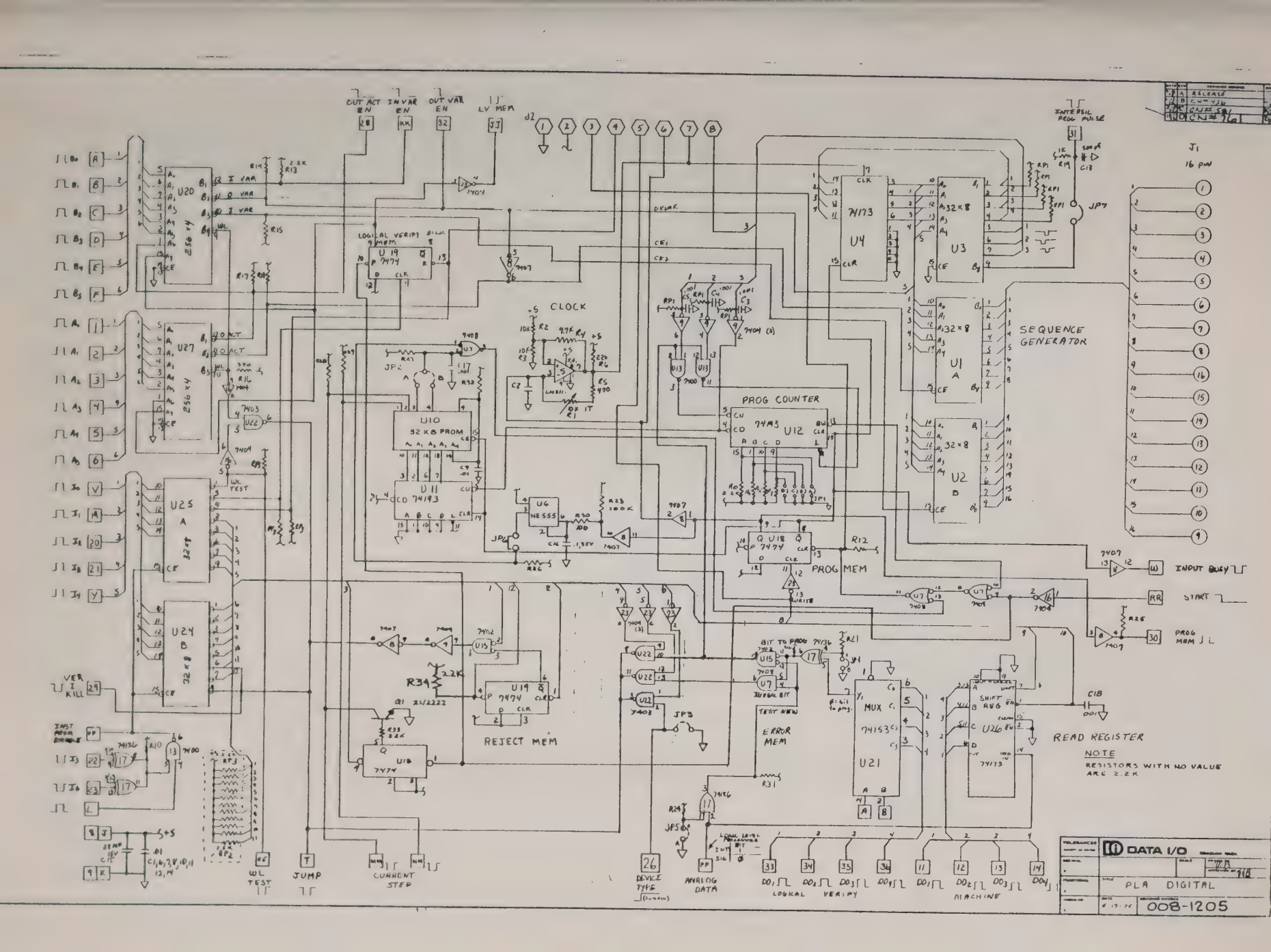
DATA I/O	
MODEL I	M.2
MOTHERBOARD	

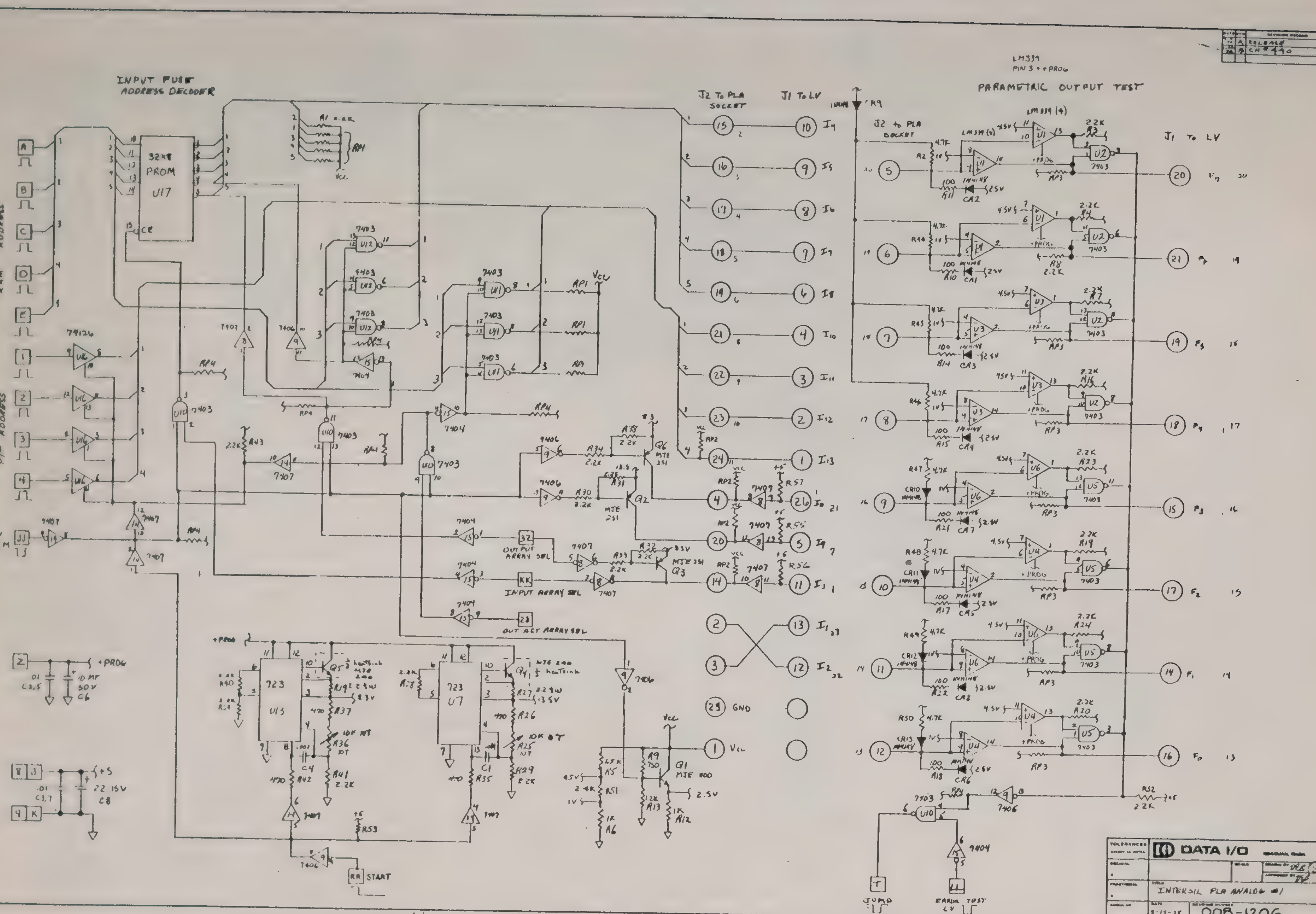

CONTROL PANEL
SELECT REGISTER
74173
STACK REGISTER
STACK COUNTER
CALL
RETURN
INC GATE
DEC GATE
COMMAND PROM CCA
COMMAND PROM CCB
INTEL 2708 INSTRUCTION PROM
INTEL 2708 JUMP SELECT PROM
JUMP GATES SELECTOR
MANUAL HALT MEM
COUNT LOAD MEM
7496
74193
DATA I/O
MODEL 3 CONTROL CARD
8/19/15
008 1201

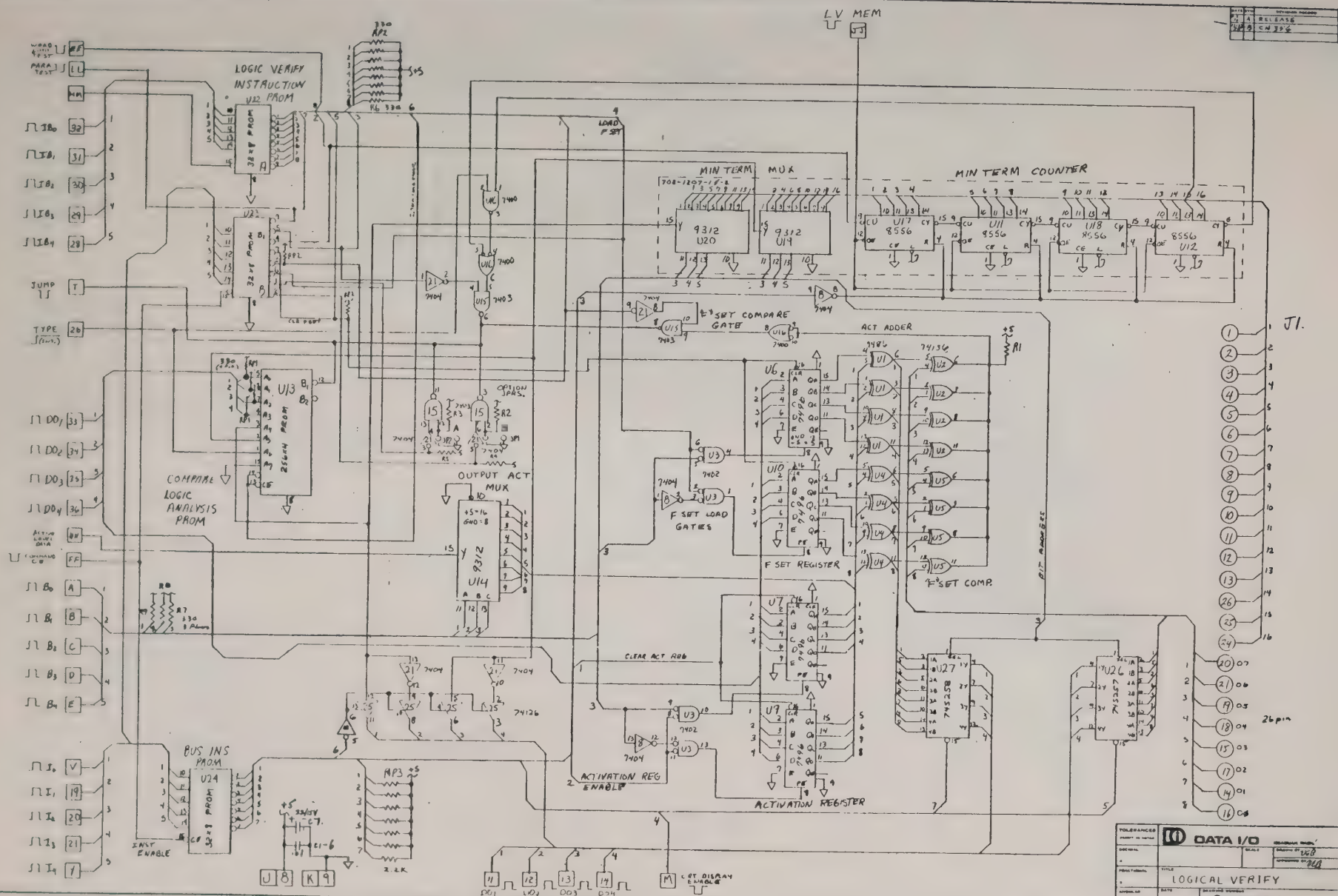

DO BUS TO LOGIC VERIFY
RESET
READ OUT GATES
74126
7407
RAM.
93415 U17
93415 U18
93415 U16
93415 U15
DO BUS REGISTER
74173
U24
STROBE GATE
7403
HIGH ORDER BIT COUNTER
74193 U9
74193 U10
74193 U11
BIT COUNTER
4 BIT COUNTER
74193 U1
HI SPEED CLOCK
7413 U14
LOGIC VERIFY RAMS
3348 U13
CLOCK MEM.
7474 U5
JP CONTROL REG.
74174 U12
3348 U19
BUFFER AMPS 7407
COMMAND PROMS
3348 U20
3348 U21
BCD-BINARY CONV.
74184 U3
74184 U4
SELECT GATE
7406
7404
COUNT 4 JUMP GATE
7474 U5
DO1
DO2
DO3
DO4
D/SYNC
I0
I1
I2
I3
I4
I5
I6
IB0
IB1
IB2
IB3
IB4
LOG VER CE
BUFFER AMPS 7407
A0
A1
A2
A3 P/T
A4
A5
B0
B1 BIT
B2
B3
B4
B5
JP EN
+5
GND
MODEL X RAM
7-30-75
008-1202
DATA I/O

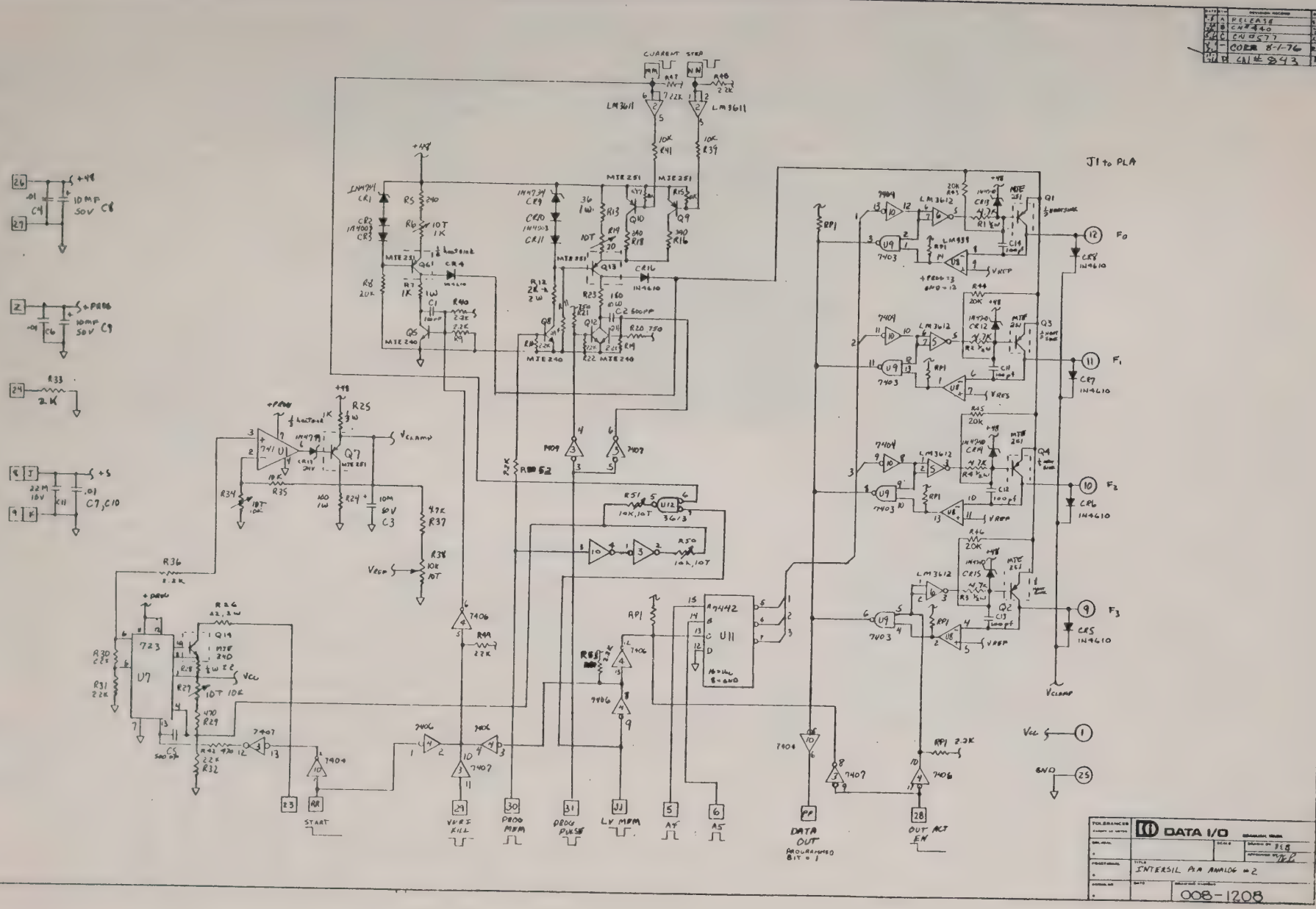

MODE SELECTION REGISTER
KEY DATA REG
COMMAND REGISTER
KEY COMMAND R/O GATES
FUNCTION SELECT ENABLE GATE
MODE R/O GATES 74126
W/R MANUAL GATE
SW DEBOUNCE CONTROL
TEST DECODER
FUNCTION SELECT REGISTER
FUNCTION R/O GATES 74126
AUTO MEM
POWER INT MEMORY
TIMER
INTERFACE CONNECTOR
RESET RAM CLEAR
POWER INTERRUPT
MODEL X CONTROL PANEL
DATA I/O
NOTE: 1. ALL RESISTORS 2.2K UNLESS NOTED

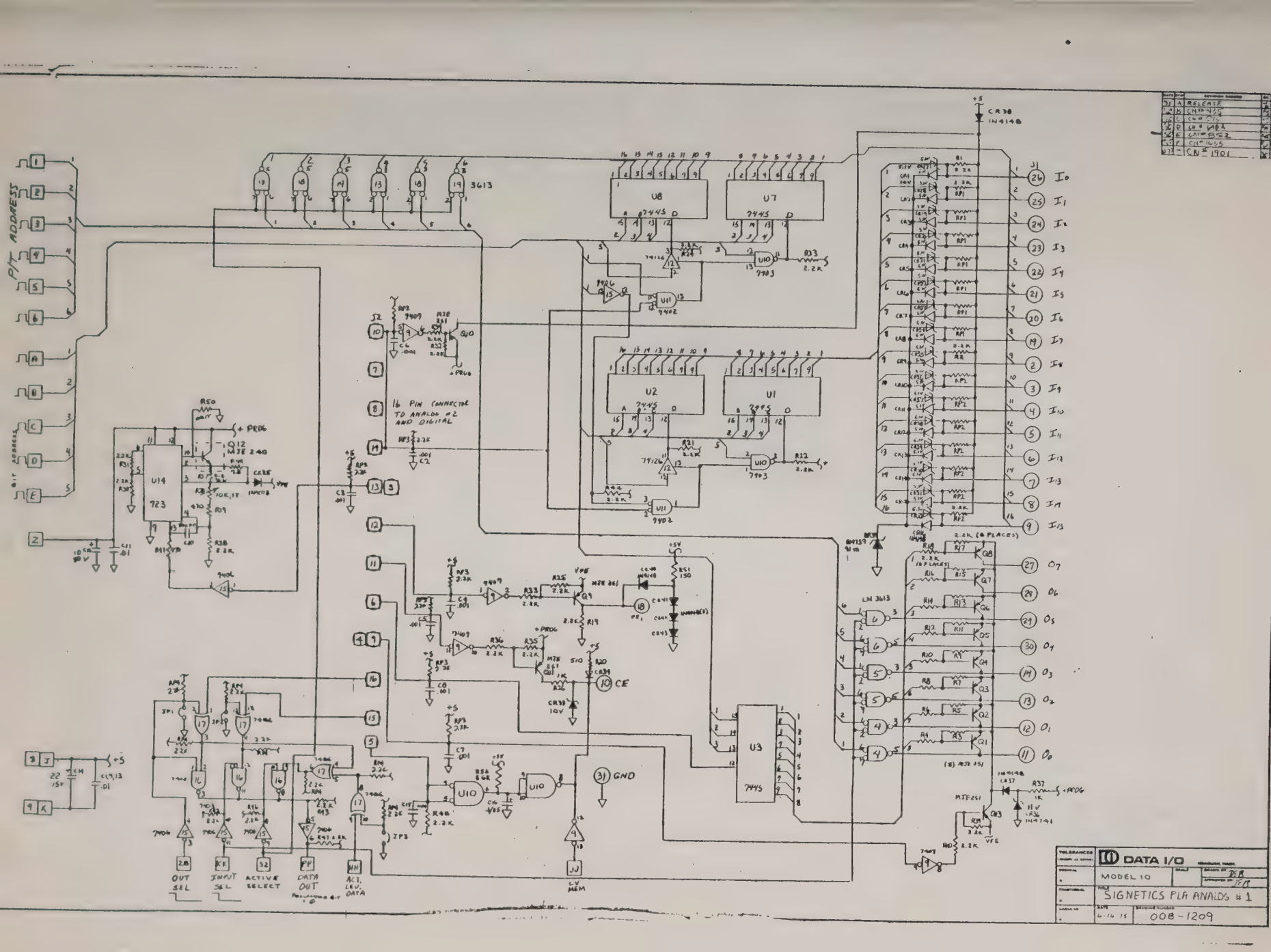

DATA DECODE
BINARY/BCD CONV
P/T LOAD GATE
DATA PROM
CRT IMAGE GATES
INSTRUCTION PROMS
FORMAT LATCH
MOS LOAD MEM
ZONE B MEM
ZONE A MEM
SECTOR GATE
SELECT GATE
CRT CLOCK GATE
LOAD COUNTER
CLOCK MEM
A MEM
B MEM
B FLAG
8 BIT DATA BUS +=BIT
MODEL X
MODEL X CRT INTERFACE
008-1204
DATA I/O

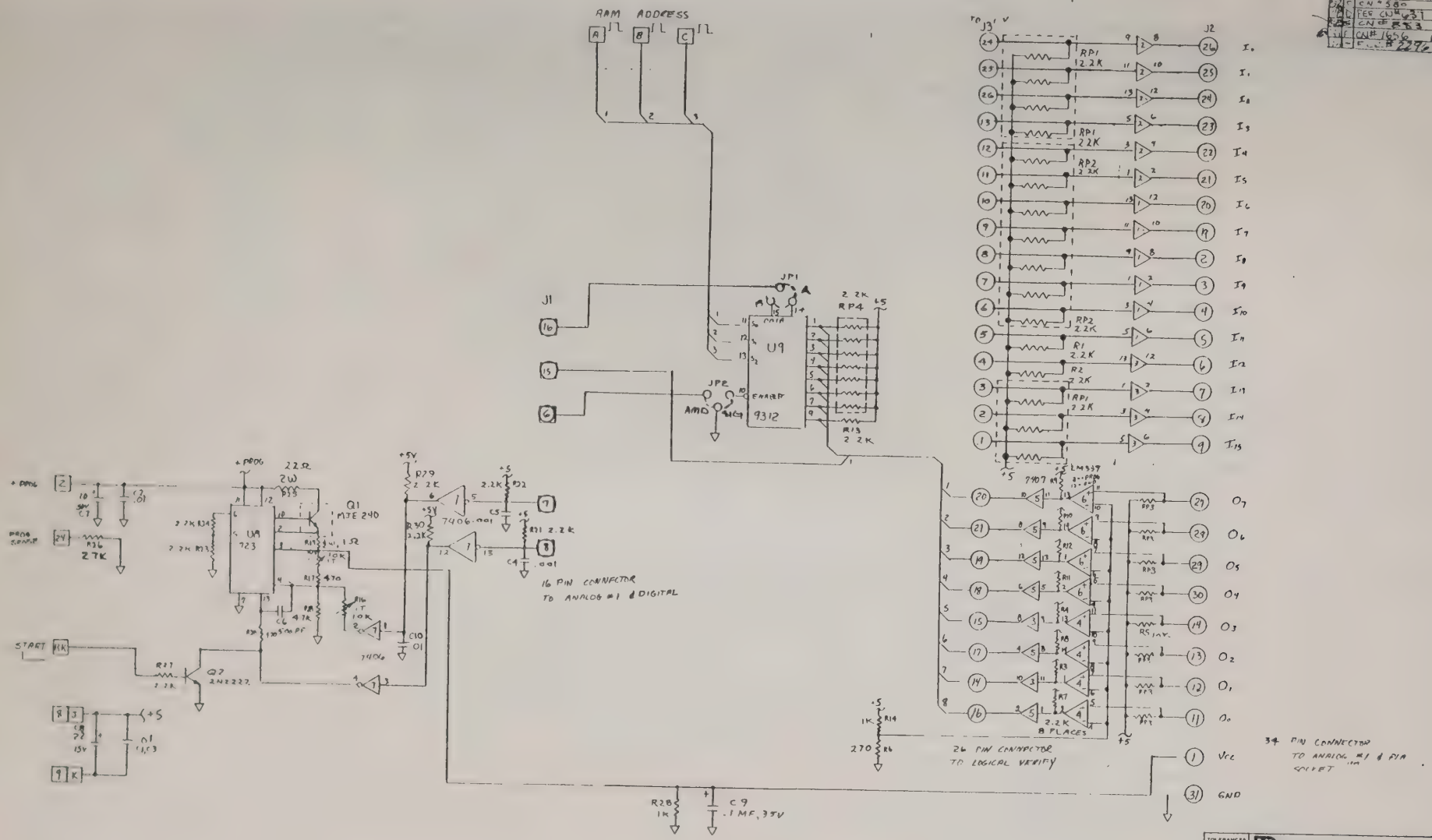

SEQUENCE GENERATOR
PROG COUNTER
PROG MEM
CLOCK
REJECT MEM
ERROR MEM
READ REGISTER
NOTE
RESISTORS WITH NO VALUE ARE 2.2K
DATA I/O
PLA DIGITAL
008-1205


INPUT FUSE ADDRESS DECODER
PARAMETRIC OUTPUT TEST
LM339
PIN 3 + PROG
J2 To PLA SOCKET
J1 To LV
RAM ADDRESS
I/T ADDRESS
LV MEM
32x8 PROM U17
OUTPUT ARRAY SEL
INPUT ARRAY SEL
OUT ACT ARRAY SEL
START
JUMP
ERROR TEST LV
GND
DATA I/O
INTERSIL PLA ANALOG #1
008-1206
RELEASE

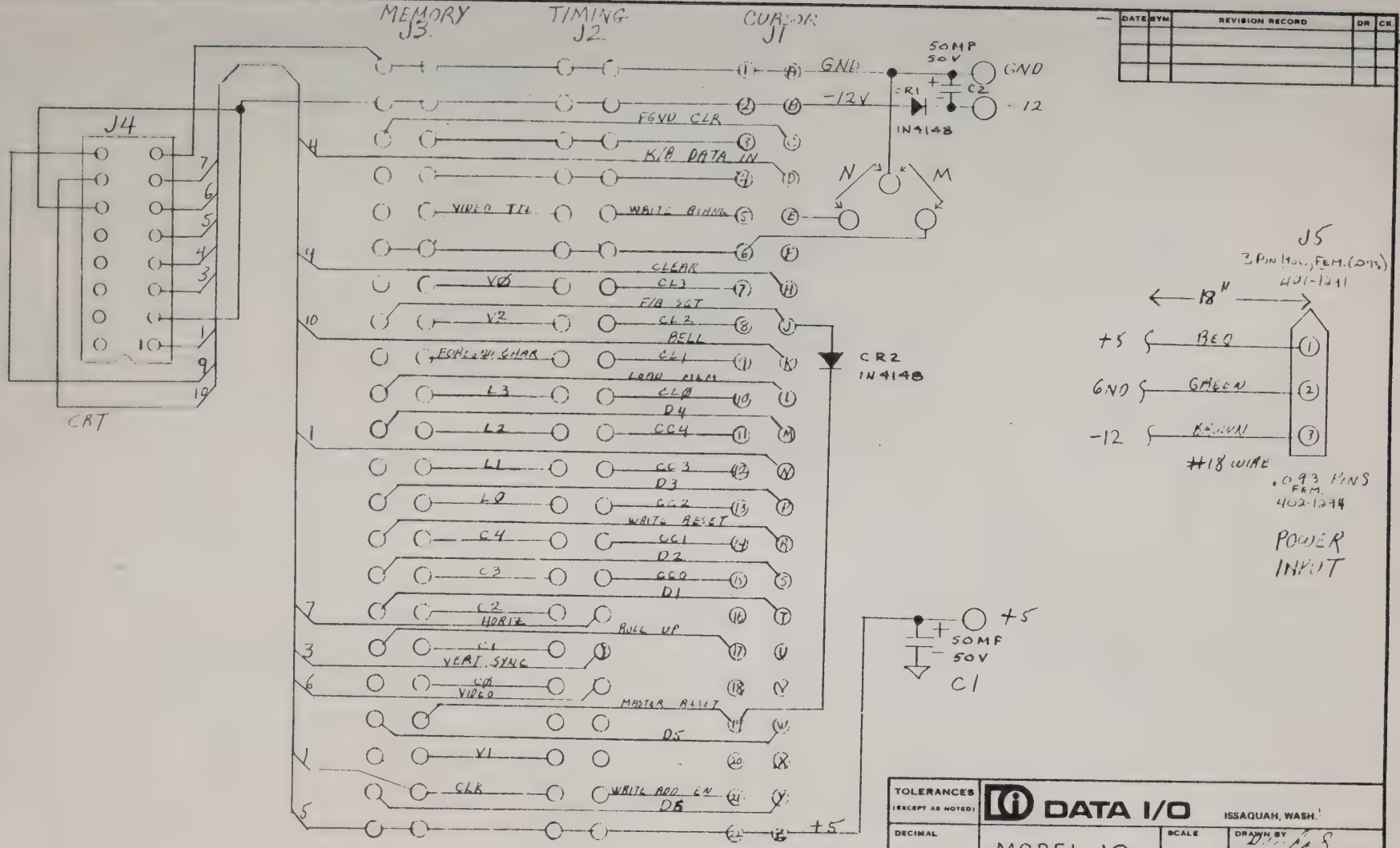

LV MEM
LOGIC VERIFY INSTRUCTION PROM
U12 PROM
MIN TERM MUX
MIN TERM COUNTER
U20
U14
U17
U11
U18
U12
LOAD F SET
F SET COMPARE GATE
ACT ADDER
OUTPUT ACT MUX
U13
COMPARE LOGIC ANALYSIS PROM
F SET LOAD GATES
F SET REGISTER
F SET COMP.
CLEAR ACT REG
ACTIVATION REG ENABLE
ACTIVATION REGISTER
BUS INS PROM
U24
INST ENABLE
SET DISPLAY ENABLE
J1.
26 pin
LOGICAL VERIFY
008-1207
DATA I/O


J1 to PLA
CURRENT STEP
LM3611
LM3611
+VPROG
+PROG
+S
VCLAMP
VREF
VCC
GND
DATA OUT
PROGRAMMED BIT = 1
OUT ACT EN
START
VERIF KILL
PROG PRM
PROG PULSE
LV PRM
A4
A5
F0
F1
F2
F3
DATA I/O
INTERSIL PLA ANALOG #2
008-1208


P/T ADDRESS
BIT ADDRESS
16 PIN CONNECTOR TO ANALOG #2 AND DIGITAL
+PROG
CE
GND
OUT SEL
INPUT SEL
ACTIVE SELECT
DATA OUT
ACT. LEV. DATA
LV MEM
DATA I/O
MODEL 10
SIGNETICS PLA ANALOG # 1
6-14-75
008-1209

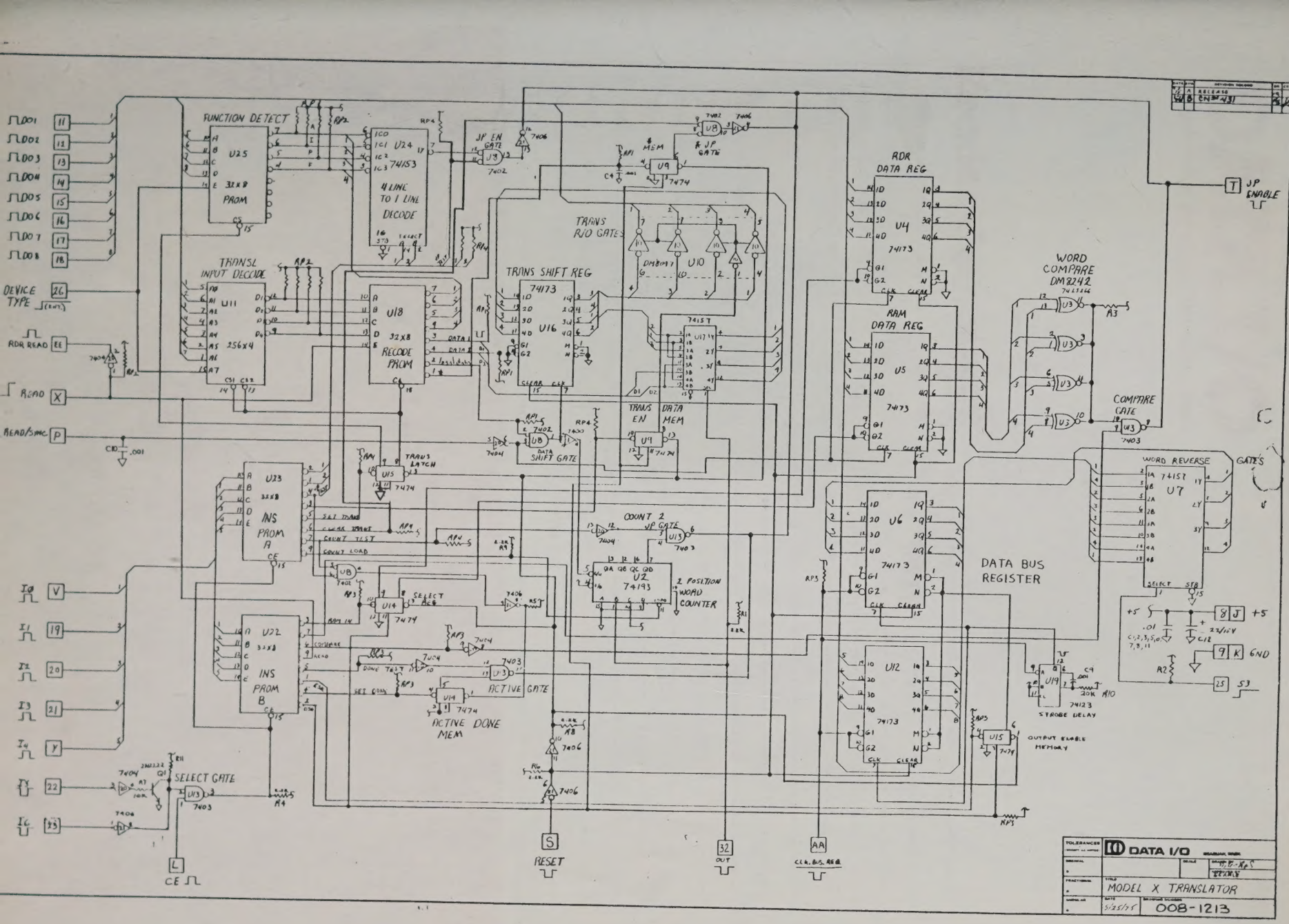


	DATA I/O	
	8	
	SIG & AMD PIA ANALOG #2	
	6-18-75	008-1210



DATE	SYM	REVISION RECORD	DR	CK

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ±	MODEL 10	SCALE	DRAWN BY DWS APPROVED BY
FRACTIONAL ±	TITLE CRT CONTROL M/B P10		
ANGULAR ±	DATE 4-10-75	DRAWING NUMBER 008-1211	


FUNCTION DETECT
U25
32X8 PROM
4 LINE TO 1 LINE DECODE
U24
74153
JP EN GATE
U9
7402
7406
JP GATE
MEM
U9
7474
TRANS RJO GATE
DM8097
U10
TRANS SHIFT REG
74173
U16
7415T
U17
TRANSL INPUT DECODE
U11
256X4
U18
32X8 RECODE PROM
TRANS DATA MEM
U9
7474
TRANS EN
SHIFT GATE
TRANS LATCH
U15
7474
INS PROM A
U23
32X8
INS PROM B
U22
32X8
SELECT ACK
U14
7474
SELECT GATE
ACTIVE GATE
U3
7403
ACTIVE DONE MEM
U14
7474
COUNT 2
UP GATE
U13
7403
2 POSITION WORD COUNTER
U2
74193
RDR DATA REG
U4
74173
RAM DATA REG
U5
74173
WORD COMPARE
DM8242
74LS266
COMPARE GATE
U3
7403
U6
74173
DATA BUS REGISTER
U12
74173
STROBE DELAY
U19
74123
20K
A10
OUTPUT ENABLE MEMORY
U15
7474
WORD REVERSE GATES
U7
74157
JP ENABLE
DEVICE TYPE
RDR READ
READ
READ/SYNC
RESET
CE
OUT
CLR. BUS. REG
+5
GND
DATA I/O
MODEL X TRANSLATOR
008-1213
5/25/75

DATA I/O
Programming systems for tomorrow...toda
92504